# Design and Fabrication of a Radiation-Hard 500-MHz Digitizer Using Deep Submicron Technology

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July 14, 2003

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# Outline

- NLC Requirements
- ADC Design
- Plans

# Beam Position Monitor Requirements at NLC

- NLC will collide 180-bunch trains of $e^-$ and $e^+$:
  - bunch spacing: 1.4 ns
  - alignment of individual bunches in a train: < 1 □m
  - BPM determines bunch-to-bunch misalignment
  - ⇨ high bandwidth kickers bring the train into better alignment on next machine cycle
  - ⇨ multi-bunch BPM system with digitizers:
    - ★ 11-bit effective resolution
    - ★ 500 MHz bandwidth
    - ★ 2 G samples/s

# Requirements of NLC Digitizers

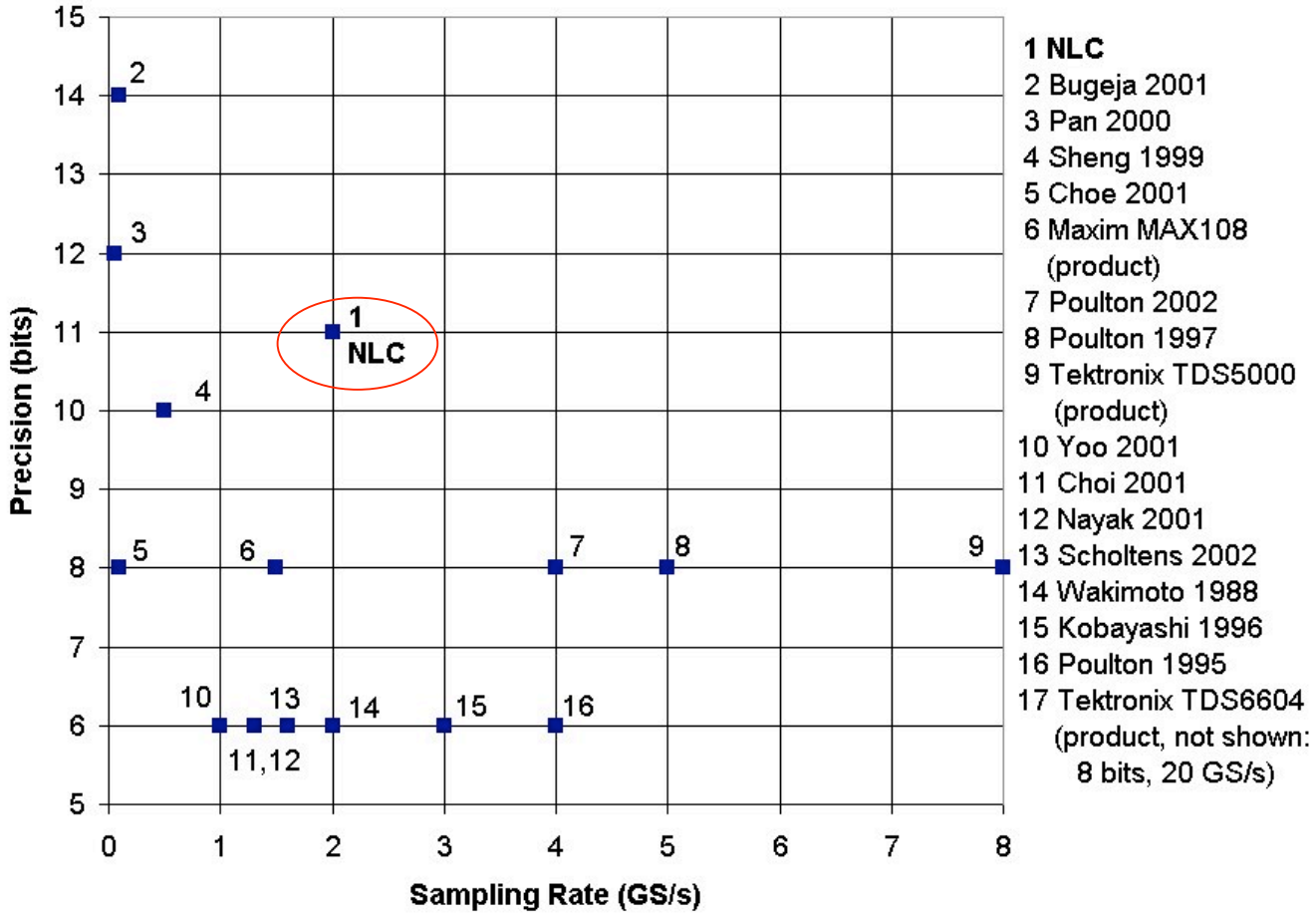
| Function | Qty. | Resolution (eff. bits) | Bandwidth (MHz) | Comments |
|---|---|---|---|---|
| LLRF Control | 13,000 | 11 | 100 | Slightly beyond state-of-the-art |
| Structure BPM | 22,000 | 8 | 5 | Existing technology |
| "Qaud" BPM | 10,000 | 11 | 12 | Existing technology |
| Multi-bunch BPM | 1,200 | 11 | 500 | Well beyond state-of-the-art |
| Total | 46,200 | | | |

- important to demonstrate feasibility of high speed/resolution digitizers
- ⇨ redesign of low level RF technology is needed without the digitizers

# Proposal

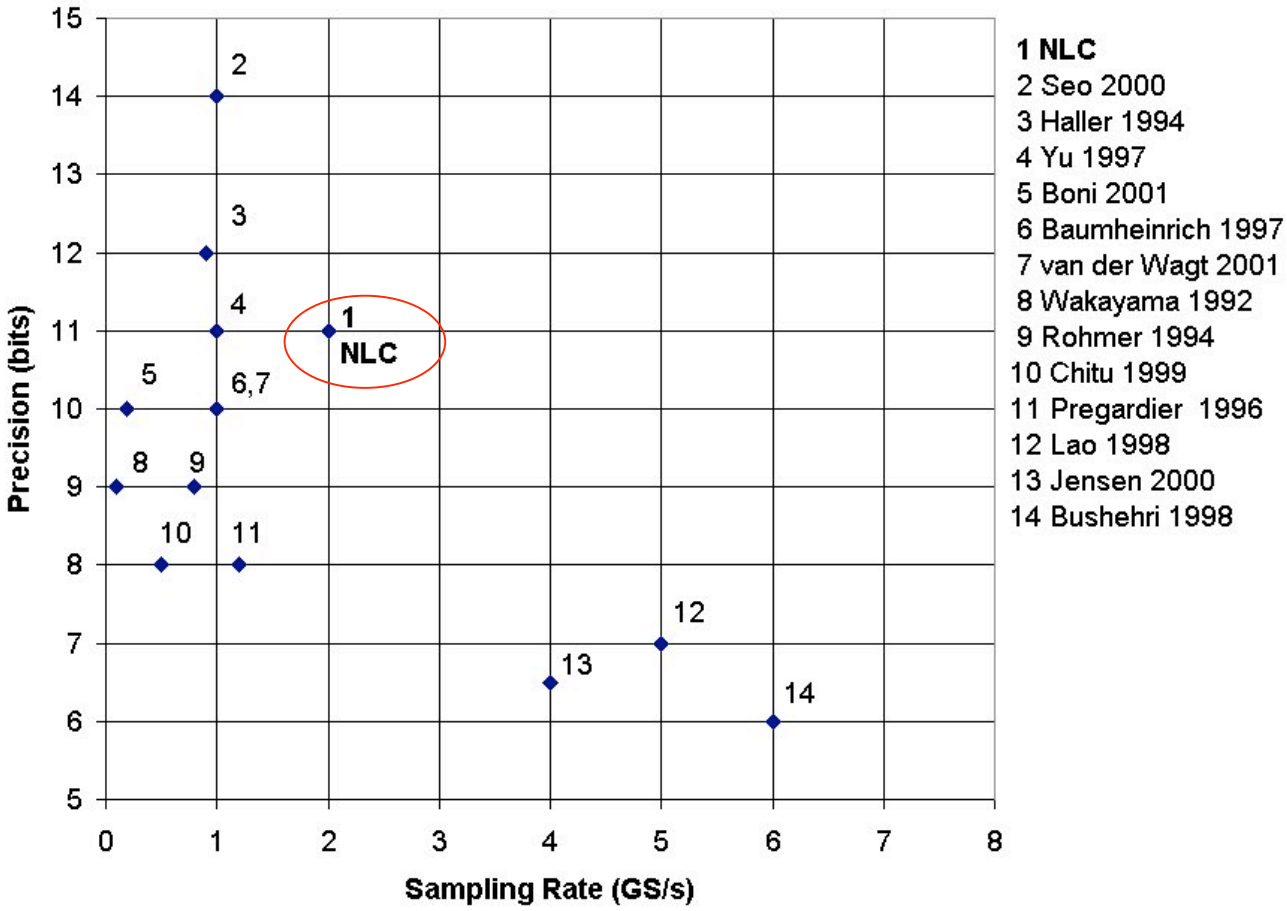
- design a digitizer chip using deep-submicron technology (0.25 □m)
  - radiation hard: > 60 Mrad
    - ⇨ no need for costly shielding and long cables
    - ⇨ readily access to electronics for testing and maintenance
- extensive experience in chip design using Cadence
  - design radiation-hard chip for CLEO III, ATLAS, CMS
- why OSU is interested?
  - help to solve a challenging NLC problem
  - potential applications in HEP
- Holtkamp Committee ranking: 2 on scale of 1 to 4 (lowest)

# Current State-of-the-Art in Digitizer




- NLC requirement is somewhat beyond state-of-the-art

# Current State-of-the-Art in Sample/Hold

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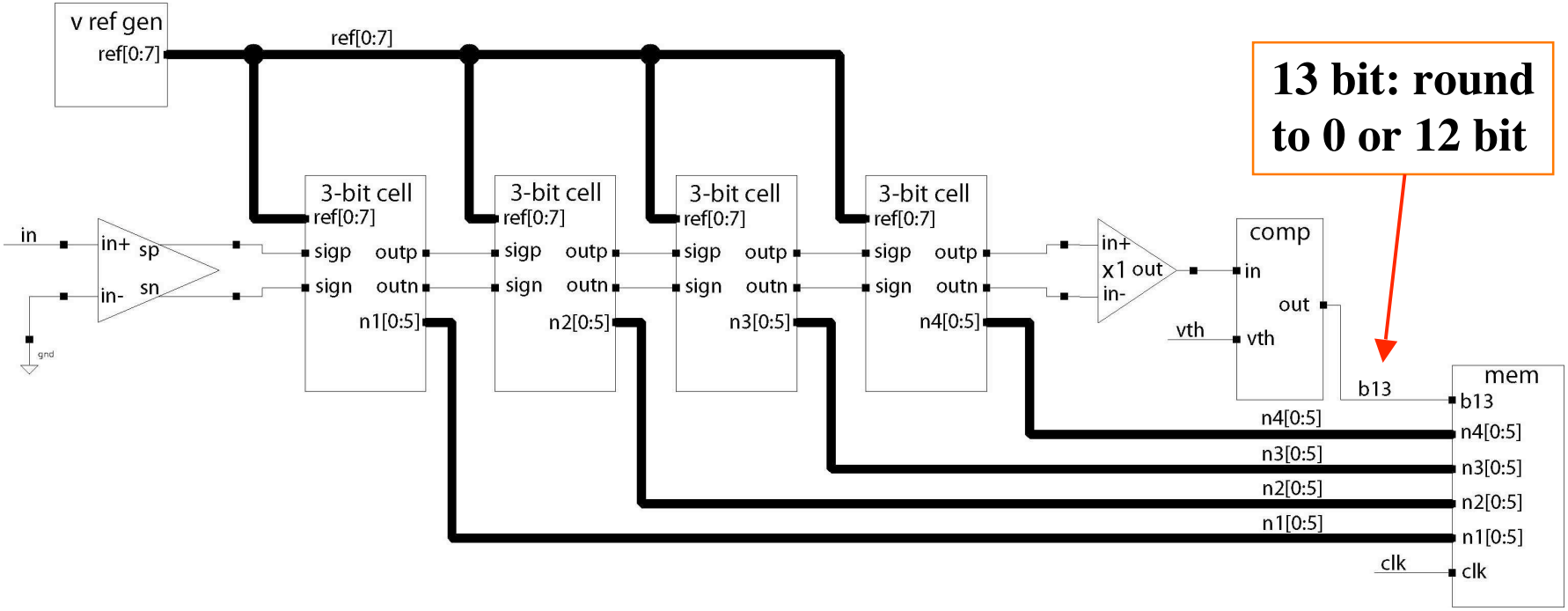
# 12-bit Pipelined Digitizer




- input crudely digitized by 1st 3-bit cell
- ⇨ digitized value subtracted from input
- ⇨ difference is amplified by 8 and send to 2nd 3-bit cell…

# Digitizer for Multi-bunch BPM

- most challenging digitizer: 11 bit, 2 G samples /s, 500 MHz bandwidth
- input: sequence of doublets at 1.4 ns batch spacing
  - characterize with one parameter: pulse height
  - minimum sampling: 1/1.4 ns = 714 MHz
    - ⇨ interleaving 3 digitizers for redundancy
      - ⇨ 2 G samples/s

# Precision

- submicron CMOS supply voltage: 2.5 V
  - ⇨ differential signal: ~ 3 V full swing
  - ⇨ LSB: 3 V/$2^{12}$ = 732 □V
  - ⇨ stability/accuracy of comparator thresholds, amplifier & S/H gains, charge injection: 366 □V = 0.5 LSB = 0.5/$2^{12}$ = 0.01%

# Error Control

- three types of errors in digitizer
  - offset: comparator thresholds, amplifiers, S/H
  - gain: amplifiers, S/H
    - ⇨ 72 calibration values for offset and gain errors to be stored into on-chip memory
  - dynamic: timing, amplifiers & S/H settling
    - ⇨ dynamic errors are controlled via careful simulation/design to ensure each circuit has sufficient bandwidth to settle in required time

# Fabrication Process

- gain-bandwidth requirement:
  - assume 0.7 ns for sample and 0.7 ns for hold
  - settling to 0.5 LSB for 12-bit digitizer requires 9□: $0.5/2^{12} \sim e^{-9}$
    - ⇨ □= 0.7 ns/9 = 171 ps
    - ⇨ gain x bandwidth = 8 x 1/2□□= 16.4 GHz
    - ⇨ IBM process SiGe BiCMOS 6HP/6DM via MOSIS: 40 GHz NPN bipolar transistors

# Plans

- require six prototypes over three years
- has been funded by DOE for design/simulation in first year
  - goal: has most circuit blocks ready
    for prototyping by end of first year