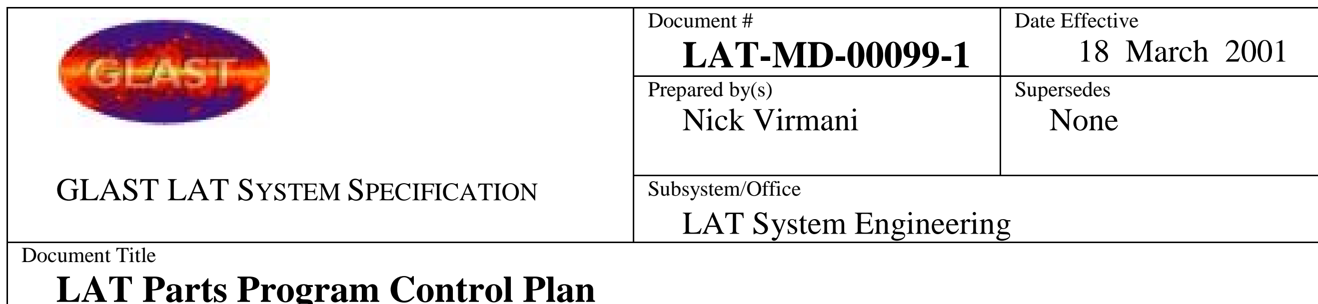

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Gamma-ray Large Area Space Telescope (GLAST)

Large Area Telescope (LAT)

Parts Program Control Plan

CHANGE HISTORY LOG

Revision	Effective Date	Description of Changes	DCN #
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1 PURPOSE

This specification describes the GLAST LAT electrical, electronic, and electromechanical (EEE) parts program. It summarizes the techniques and methods by which the EEE parts program achieves maximum part reliability within cost and schedule constraints. The EEE parts program will ensure that all parts used are of the highest level of reliability available consistent with their functional requirements, as well as program cost and schedule constraints. As a goal, GLAST LAT designs will use quality level 2 parts as per GSFC-311-INST-001, minimizing the number of parts type combinations, and minimizing duplicate specifications, and duplicate procurements actions. It describes the selection, screening, and monitoring of EEE parts used in the hardware being built by subcontractors, vendors, or collaborators and Naval Research Laboratory (NRL). The purpose of this document is to define criteria for selecting screening and qualification of EEE parts intended for GLAST LAT mission. This will assist project manager and subcontractor, vendor, or collaborator to develop effective EEE parts program, based on mission reliability objective. An alternative qualification plan may be considered, provided it meets the intent of GSFC-311-INST-001, and a significant cost savings be realized. The subcontractor, vendor, or collaborator shall submit alternate plan to GLAST LAT Parts Control Board (PCB) for approval. The GLAST LAT PCB has the primary responsibility of conducting the parts and materials program for space flight parts. Should there be a conflict between this document and the contract, the contract shall take precedence. Should there be a conflict between this document and another document, this document shall take precedence.

The EEE program will be based on the evaluation of the following three critical reliability factors:

- The materials and processes employed in a device's manufacture;
- The tests and inspections to which a device is subjected; and
- The electrical and environmental stresses experienced in a device's application.

The part reliability enhancement, assurance techniques and methods defined herein address five major activities that comprise the HI-REL parts program. These activities are:

- Parts Program Management Approach
- Parts Selection, Derating and Qualification
- Parts Procurement and Screening
- Destructive Physical Analysis
- Quality Assurance Provisions

2 SCOPE

This plan establishes the requirements of GLAST LAT EEE parts baseline and is based on the requirements specified in GLAST LAT Mission Assurance Requirements (MAR) dated Oct. 26, 2000 and NASA 311-INST-001, Rev. A, Quality level 2 (hereon referred to as 311-INST-001) except as specified herein or allowed by the PCB. All part types listed in the GSFC PPL-21 along with Motors, Application Specific Integrated Circuits (ASICs), Multi-Chip Modules (MCM), High Density Interconnects (HDI), Detectors, and Charge Coupled Devices (CCD) are considered EEE parts and shall be subject to GLAST LAT PCB control.

3 DEFINITIONS

3.1 Acronyms

GLAST	Gamma-ray Large Area Space Telescope
IRD	Interface Requirements Document
LAT	Large Area Telescope
PI	Principal Investigator

SI/SC IRD	Science Instrument – Spacecraft Interface Requirements Document
SRD	Science Requirements Document
TBR	To Be Resolved

3.2 Definitions

γ	Gamma Ray

4 APPLICABLE DOCUMENTS

The following documents of the issue in effect, at the time of the GLAST LAT support program, form a part of the requirements of this control plan, to the extent referenced herein. If there is any conflict between this document and the documents listed herein, this document will take precedence.

4.1 DOCUMENTS

GSFC-311-INST-001	Goddard Space Flight Center Instructions for EEE Parts Selection, Screening and Qualification.
GSFC-PPL-21	GSFC Preferred Parts List (http://epims.gsfc.nasa.gov)
GSFC-S-311-M-70	Specification for Destructive Physical Analysis (DPA)
GSFC-TR04-0600	Plastic Encapsulated Microcircuit Derating, Storage and Qualification Report
MIL-STD-883	Test methods and procedures for Microelectronics
MIL-STD-975	NASA Standard Electrical, Electronics and Electromechanical (EEE) parts list
MIL-PRF-19500	Semiconductor Devices, General Specification for
MIL-M-38510	Microcircuits, General Specification for
MIL-PRF-38534	Hybrid Microcircuit, General Specification for
MIL-PRF-38535	Microcircuits Manufacturing, General Specification for
NASA Reference Publication (RP) 1124	Outgassing Data for Selecting Spacecraft Material
NHB 8060.1	Flammability, Odor and Offgassing Requirements and Test Procedures for Materials in Environments that Support Combustion
NASA Parts Selection List (NPSL)	Part Derating Guidelines (http://nepp.nasa.gov)
433-SPEC-0001	Gamma-Ray Large Area Space Telescope (GLAST) Project Mission System Specification
OTHER PUBLICATIONS	
Electronic Industries Association (EIA)	
JESD 22-A102	Accelerated Moisture on unbiased Autoclave
JESD 22-A101	STEADY-STATE TEMPERATURE HUMIDITY BIAS LIFE TEST

JESD 22-A104	TEMPERATURE CYCLING
JESD 22-A108	TEMPERATURE, BIAS, AND OPERATING LIFE
JESD 22-A110	HIGHLY ACCELERATED TEMPERATURE AND HUMIDITY STRESS TEST (HAST)
JESD 22-A113-A	PRECONDITIONING OF PLASTIC SURFACE MOUNT DEVICES PRIOR TO RELIABILITY TESTING
JEDEC STANDARD 26	PROPOSED GENERAL SPECIFICATION FOR PLASTIC ENCAPSULATED MICROCIRCUITS FOR USE IN RUGGED APPLICATIONS
IPC/JEDEC J-STD-020A	MOISTURE REFLOW SENSITIVITY CLASSIFICATION
IPC/JEDEC J-STD-033	STANDARD FOR HANDLING, PACKING, SHIPPING, AND USE OF MOISTURE/REFLOW SENSITIVE SURFACE MOUNT DEVICES
IPC/JEDEC J-STD-035	ACOUSTIC MICROSCOPY FOR NON-HERMETIC ENCAPSULATED ELECTRONIC COMPONENTS
ANSI /IPC-SM-786	RECOMMENDED PROCEDURES FOR HANDLING OF MOISTURE SENSATIVE PLASTIC IC PACKAGES
American Society For Testing And Materials (ASTM0)	
ASTM-E-595	Standard Test Method for Total Mass Loss and Collected Volatile Condensable Material from Outgassing in a Vacuum Environment

5 PARTS PROGRAM MANAGEMENT

5.1 ORGANIZATION

The GLAST LAT Project Parts Engineer (PPE) has responsibility for the parts program. Parts Engineering of GLAST LAT along with GLAST LAT PCB maintains direct control of the selection, screening, and qualification of all EEE parts per section 6.0 of this document. Subcontractors, vendors, or collaborators involved in building flight hardware will document the approach and capability to manage and control the EEE parts program. This document will include all QA provisions and part stress analysis for evaluating circuit design, conformance to derating guidelines and requirements of this document.

6 EEE PARTS SELECTION, SPECIFICATION, STANDARDIZATION, AND QUALIFICATION

All EEE parts will be selected and processed in accordance with GSFC 311-INST-001: "Instructions for the EEE Parts Selection, Screening and Qualification". All application notes in 311-INST-001 of quality level 2 will apply. The part quality level 2 defined in 311-INST-001will apply to this program as determined by the Project Manager. The requirements of 311-INST-001 may be further tailored as appropriate and shall be subjected to PCB approval. Parts selected from the NASA Parts Selection List (NPSL) http://nepp.nasa.gov, MIL-STD-975, and the GSFC Preferred Parts List (PPL-21) are considered to have met all criteria of 311-INST-001, quality level 2, and may be approved by the PCB provided all mission application requirements (performance, derating, radiation, etc.) are met and need not be subjected to additional screening, qualification or QCI tests.

6.1 PARTS SELECTION CRITERIA

Parts for use on the program shall be selected in the order of preference as listed in the following paragraphs. Parts falling into the categories for paragraphs 1 through 9 need not be subjected to any additional screening, qualification, or QCI tests. Parts falling into the categories for paragraphs 10 through 12 may require additional

testing to be in conformance with the requirements of 311-INST-001. In all cases, the radiation hardness characteristics (Total Ionizing Dose (TID), Single-Event Upset (SEU), and Single-Event Latch-up (SEL)) should be established and implemented. Particle Impact Noise Detection (PIND) testing shall be performed on all cavity devices as outlined in section 6.10 of this document.

1. Parts listed in the GSFC Preferred Parts List (PPL-21), MIL-STD-975 or with previous space flight heritage. Parts will be procured in accordance with the appropriate specification designated for that part.
2. MIL-M-38510, Class B or better microcircuits procured from a Qualified Products List (QPL) supplier. MIL-M-38510, class B microcircuits do not require lot specific 1000 hour life test. http://www.dscc.dla.mil/offices/sourcing_and_qualification and http://www.dscc.dla.mil/offices/doc_control.
3. MIL-PRF-38535, Class Q or better microcircuits procured to standard military drawings (SMDs) from a supplier listed in the Qualified Manufacturer List (QML) at http://www.dscc.dla.mil/offices/sourcing_and_qualification and http://www.dscc.dla.mil/offices/doc_control.
4. MIL-PRF-38534, Class H or better hybrid microcircuits, procured from a supplier listed in the Qualified Manufacturer List (QML), and with additional screening, if necessary.
5. Microcircuits compliant with paragraph 1.2.1 of MIL-STD-883 and procured from manufacturers having QPL or QML status for parts of the same technology. Parts procured from manufacturers without QPL or QML status will be procured with lot specific or generic Group C Quality Conformance Inspection (QCI) data within one year of the lot date code of the part being procured. These parts will be subjected to additional screening as per GSFC 311-INST-001, quality level 2.
6. Manufacturers in house reliability processed parts, provided all screening tests listed in GSFC 311-INST-001 for a quality level 2 part has been satisfied. The high reliability process flow shall be formally documented by the manufacturer in cases where changes would require a revision to the flow documentation. Tests not included in the manufacturer's reliability flow must be performed by the PPE at an independent test facility or at GSFC or by the subcontractor, vendor, or collaborator. Parts shall be procured following this guideline with lot specific or generic group C Quality Conformance Inspection (QCI) data and shall be approved by the Part Control Board (PCB).
7. MIL-PRF-19500, JANTX, JANTXV and JANS semiconductors procured from a QPL listed supplier and screened per GSFC311-INST-001. DPA required for JANTX/JANTXV level parts per GSFC311-INST001 will be evaluated by the Part Control Board (PCB) on a case-by-case basis. It is preferred that semiconductors be procured to JANTXV level or better.
8. Established Reliability (ER) passive components procured from a QPL listed supplier for the appropriate military specification. Part failure rates should be in accordance to the guidelines in GSFC-311-INST-001 for a quality level 2 part. Also parts values should be within the minimum and maximum ranges specified in PPL-21.
9. Parts previously approved by GSFC via the Nonstandard Parts Approval Request (NSPAR) on previous flight missions for a system similar to the one being procured will be evaluated by the PCB for continued compliance to current project requirements prior to listing in the Project Approved Parts List (PAPL). This will be accomplished by determining that:
    a. Non-changes have been made to the previously approved NSPAR, Source Control Drawing (SCD), or vendor list.
    b. All stipulations cited in the previous NSPAR approval have been implemented on the current flight lot including performance of any additional testing.
    c. The previous project's parts quality level is identical to the current project.
10. Any parts not meeting the criteria specified in paragraphs 1 through 9 above shall be screened in accordance with the screening requirement specified in 311-INST-001, quality level 2 for each commodity. Changes in form, fit, function, reliability or manufacturer shall be cause to require improving the screening

of a PCB approved heritage part to meet the screening requirement of 311-INST-001, quality level 2 for each appropriate commodity.

11. Plastic Encapsulated Microcircuits (PEMs) should be the exception rather than the rule. If a part is available in a hermetic package and plastic package, the hermetic package will be used. All PEM shall be qualified in accordance with the qualification requirements specified in 311-INST-001, quality level 2.
12. Precap inspection at subcontractor, vendor, or collaborator's facilities will be performed on hybrid microcircuits (dc/dc converters) and other complex microcircuits, such as a custom gate array, or an Application Specific Integrated Circuit (ASIC), multichip modules, and 3-D stacks.

These specifications for these EEE parts shall identify the part being procured and shall include physical, electrical, and environmental test requirement and quality assurance provisions necessary to control manufacture and acceptance. Screening requirements designated for the parts can be included in the procurement specification. 311-INST-001 and GLAST LAT parts program control plan shall be used as a reference document while preparing part specifications and source control drawings when required. For Lot acceptance or rejection, the Percentage of Defectives Allowable (PDA) in a screened lot shall be in accordance with that prescribed in the closest military part specification.

These documents shall be submitted to the PCB for approval, prior to the scheduled procurement of the part on GLAST LAT. All parts approved as per 6.1 paragraph 10 through 12 shall receive 100% screening in accordance with 311-INST-001, quality level 2 for each appropriate commodity. Requirement of 311-INST-001 shall be specified in the procurement documents.

6.2 PARTS SPECIFICATION

All EEE parts shall be procured in accordance with military, NASA, or GLAST LAT controlled specifications as specified in 311-INST-001, quality level 2, except as noted herein.

6.3 PARTS QUALIFICATION

All EEE parts shall be qualified in accordance with the qualification requirements specified in 311-INST-001, quality level 2, for each appropriate commodity, with the following exceptions:

a. Parts procured to military specifications having a QPL or QML listing status, and listed in the GSFC PPL or MIL-STD-975 as grade 2 are considered qualified and require no further qualification or QCI testing (example: MIL-M-38510, Class B microcircuits do not require lot specific 1000 hour life test).

6.4 EEE PARTS SCREENING

All newly approved parts shall be screened in accordance with the screening requirements specified in 311-INST-001, quality level 2 for each appropriate commodity. Changes to form, fit, function, reliability or manufacturer shall be cause to require improving the screening of a PCB approved heritage part to meet the screening requirement of 311-INST-001, quality level 2 for each appropriate commodity.

6.5 HYBRIDS, PIN PHOTODIODE, MCM, ASIC AND OTHER ADVANCED MICROCIRCUITS.

Hybrids and MCMs shall b designed and procured in accordance with the requirements of MIL-H-38534, device class H or equivalent. ASIC and other advanced microcircuits shall be designed and procured in accordance with MIL-PRF-38535, device class Q or equivalent. The PCB shall be responsible for assurance that 311-INST-001, level 2 requirements are met for those microcircuits that are not listed on the QPL or QML.

6.6 CUSTOM MICROCIRCUIT DEVICES

Custom hybrids or microcircuits planned for use on this GLAST LAT spaceflight program shall be subject to a design review. The review shall follow standard design review procedures and shall, as a minimum, address issues

of derating of elements, method used to assure each element is of the appropriate quality level, and method used to assure adequate thermal matching of materials. The design review could be included as part of a PCB meeting, however, the appropriate NASA/GSFC representative shall be notified of the design review with sufficient advance notice to allow for them to participate in the review.

6.7 DESTRUCTIVE PHYSICAL ANALYSIS (DPA)

A Destructive Physical Analysis shall be performed on samples of each lot of microcircuits, hybrid microcircuits, and semiconductor devices. DPA test, procedures, sample size, and criteria will be as specified in GSFC specification S-311-M-70, Destructive Physical Analysis. DPA will be performed as per S-311-M-70 and will be submitted to the PCB. Variation to the DPA shall be evaluated and approved by the PCB on a case-by-case basis. In lieu of performing the required DPA's, the LAT PPE may provide the required number of DPA samples to GSFC for DPA. The LAT PPE and GSFC will accomplish this on a case-by-case basis through mutual agreement.

6.8 ALERTS (GIDEP, NASA ADVISORIES)

The LAT PPE will be responsible for the review and disposition. As a member of Government Industry Data Exchange Program (GIDEP) Alerts for applicability to the parts proposed for use or incorporated into the design. In addition, any NASA Alerts and Advisories provided to the GLAST LAT Project by GSFC via the EEE Parts Information Management System (http://misspiggy.gsfc.nasa.gov), will be reviewed and dispositioned. The LAT PPE shall submit responses to the PCB on the applicability of the problem for the project usage, the hardware or software that is affected, part location, and the actions to be taken.

6.9 SUBCONTRACTOR, VENDOR, OR COLLABORATOR CONTROLS

The applicable requirements of this plan will be flowed down to subcontractors, vendors, or collaborators. Each subcontractor, vendor, or collaborator will be evaluated for Parts Program compliance. This evaluation will include verification of processes, for example, "Selection of Outside Test Facilities". All noncompliance to these requirements will be documented and disposition in PCB minutes for approval. The subcontractor, vendor, or collaborator will include parts program control as part of each design review and shall be submitted through the LAT PCB.

6.9.1 Subcontractor, vendor, or collaborator Data Items

Formal submittal of the following documents is required.

1. EEE parts list will be submitted by hard copy and electronically. It will contain a minimum of:
    1. Generic part number.
    2. Whether it is a standard or nonstandard part.
    3. PCB approval date.
    4. Flight part number.
    5. Manufacturer name.
    6. Indication that part has been evaluated for radiation compliance.
    7. Source limitations.
2. Part Stress Analysis
3. Radiation analysis, including part level radiation based on wall thickness and design margin compliance and SEEs analysis relative to Single-Event Upset (SEU), latchup, gate rupture, and so on, and the box-level impact.
4. List anticipated outside test facilities that would be performing tasks such as screening, qualification, and DPA on EEE parts.

5. Part drawings or specifications that provides screening and/or qualification criteria and all revisions.

6.10 PARTICLE IMPACT NOISE DETECTION (PIND) TEST

All EEE parts with internal cavity will be subjected to PIND testing in accordance with GSFC 311-INST-001. PIND testing will be done by the parts manufacturer as part of the screening flow or by LAT PPE after receipt of the parts, per GSFC 311-INST -001 for a quality level 2 part. Based on the result of the analysis, the PCB will accept or reject these lots.

6.11 DERATING

Derating is a method of reducing stress and/or making quantitative allowances for a part's functional degradation. Consequently, derating is a means of reducing failures, extending part life, and increasing reliability. In addition, derating help protect parts from unforeseen application anomalies and overstresses.

The following definitions will be used while derating parts:

1. Derate – to reduce the voltage, current, or power rating of a part to improve its reliability or to permit operation at high ambient temperatures.
2. Derating – The reduction in rating of a part especially the maximum power-dissipation rating at higher temperatures.
3. Derating Factor – The factor by which the ratings of parts are reduced to provide additional safety margins in critical applications or when the parts are subjected to worst GLAST LAT environmental conditions for which their normal ratings do not apply.

All parts after derating must meet safety, mission, and performance requirements including functionality and reliability. No part should exceed its maximum rated power conditions. That being voltage, current, thermal resistance and junction temperature. Temperature related parameters could be adjusted down or controlled to meet performance temperature requirements. Part stress analysis must verify that the derating requirements are met and documented on schematics.

All EEE parts will be derated in accordance with the derating guidelines of the NASA Parts Selection List, which is listed on the NASA Electronic Parts and Packaging Program web site http://nepp.nasa.gov, PPL-21. See Appendix A for derating guidelines for hermetic devices based on PPL-21 and Appendix B for PEM parts based on GSFC-TR04-0600.

The PEMs will meet the performance and reliability criteria established for their application when used. Two methods of derating PEMs are:

1. By reducing heat and electrical stress
2. By compensating for functional loss.

Heat and electrical stress derating are applied to the voltage, current, and power stresses of the microcircuit. Functional loss and/or performance degradation over the part's life requires a degree of parametric derating. Derating will be applied knowledgeably and only enough to improve reliability, and only once throughout the application cycle. The severity of an application and its environment will also be used as additional criteria for derating.

Tables 1 through 5 in Appendix B, as per GSFC-TR04-0600, details the type (technology-product), deration parameters, and maximum allowable limits (percentage and/or temperature) of operation (in specific environment) for the PEM microcircuits.

6.12 PARTS STRESS ANALYSIS

Electrical stress analysis is the process of determining a part's ability to withstand induced stresses under GLAST program environmental conditions. Induced stresses are taken from the datasheet and circuit analysis, and are

identified in terms of voltage, current, power, etc. Environmental conditions refer primarily to temperature and will be taken from the system's operating requirements.

Electrical circuits will be analyzed to determine the maximum stress on each part when all applied voltages or currents are maximized and when all variations of other parts in the circuit are set to that combination of minimum and maximum values that produce worst-case maximum stress. This may require a new choice of "other" part combinations in the circuit each time the stress on a new part is determined. Imposing maximum operating temperature when comparing the part stress to its required derating will aggravate the stresses. The initial analysis usually will be made without benefit of a detailed part level thermal analysis; therefore a conservative temperature assumption will be made. Highly stressed parts will be identified for possible replacement for more robust parts or for possible circuit changes. The final design will be confirmed by analysis, with part temperatures based on a part level thermal analysis, and with voltages and currents derived from either specification limits or the results of worst-case circuit analysis.

6.12.1 Stress Analysis Procedure

Prior to performing a stress de-rating analysis, a thermal analysis and circuit analysis will be completed. Circuit analysis is considered outside the scope of this document. In brief, circuit analysis is the process used to calculate the electrical parameters of each part in the circuit, such as voltage, current, power, etc. After thermal and electrical parameters are known, it is possible to calculate part stress ratings. The part stress rating is defined as the ratio of applied to rated electrical parameters. These electrical parameters may consist of voltage, current, power, inverse voltage, etc., or any combination, depending on the part.

The next step in the electrical stress derating analysis process is to calculate the stress ratios and document the results of the stress analysis. The stress ratio is the numeric ratio between the actual stresses determined from the circuit analysis divided by the stress rating of the part at the operating temperature.

The best method to document a stress analysis is usually through a worksheet or spreadsheet that allows for a logical flow of information from left to right with all required data and parameters specifically called out in columns. This obviates the casual omission of required parameters. The analysis is most effectively accomplished with the use of different worksheets for the various part categories. Typical examples of worksheets are contained in the Appendix C containing Tables 1 through 6.

6.13 PARTS AGE CONTROL

Parts drawn from controlled storage more than 5 years, after their last documented screening will be submitted to the PCB for approval. Re-screening per GSFC 311-INST-001 for quality level 2 parts might be required. Parts stored in uncontrolled conditions or exposed to the elements or sources of contamination will not be used. Subcontractor, vendor or collaborator shall submit the parts storage plan/document to PCB for approval for waiving the requirement of screening if the parts are stored in controlled environment.

6.14 RADIATION HARDNESS

A radiation evaluation to the GLAST LAT program unique radiation environment, as outlined here, will be performed on all EEE parts using as a reference, the GSFC Radiation Effects and Analysis Database (http://flick.gsfc.nasa.gov/radhome.htm), the Space Environment and Effects Program (http://see.msfc.nasa.gov), and the NASA Electronics Radiation Characterization Project Homepage (http://erc.gsfc.nasa.gov). All EEE parts will be selected to meet the following GLAST LAT mission radiation environment (Ref. 433-SPEC-0001). The radiation environments consist of two separate effects, the Total Ionizing Dose (TID) and the Single-Event Effect (SEE).

The TID for a 5-year mission in the GLAST orbit, beginning 2005, is given by the dose-depth curve in figure 1 (Ref. 433-SPEC-0001).

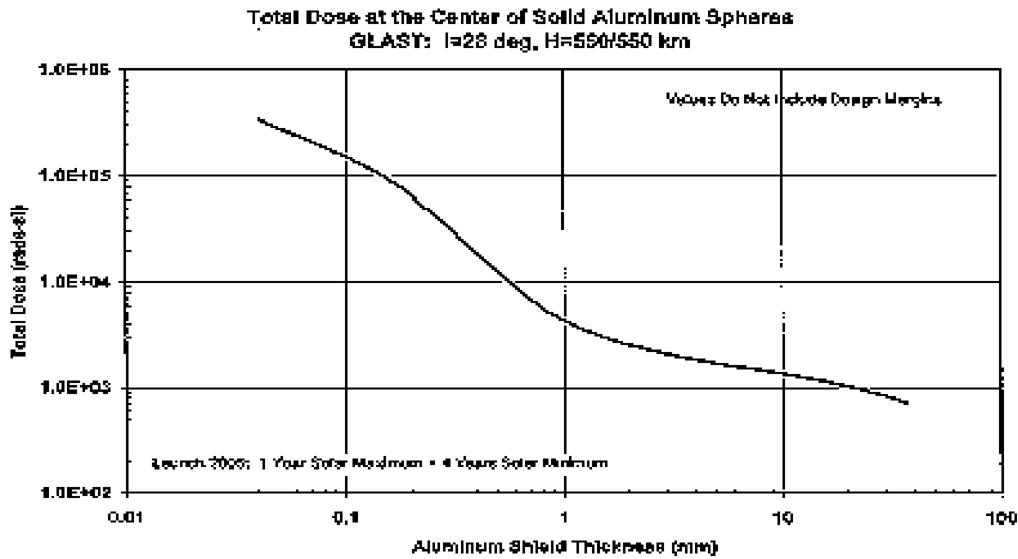


Figure 1. Total Dose-Depth Curve

A multiple factor of 2 shall be applied to the total dose estimate for estimate uncertainty, and an additional factor of 2.5 (TBR) shall be applied to achieve an overall design margin of 5. Shielding shall be designed and parts chosen to yield the required design margin.

The Linear Energy Transfer (LET) Spectrum for direct ionization by heavy ions is given in figure 2.

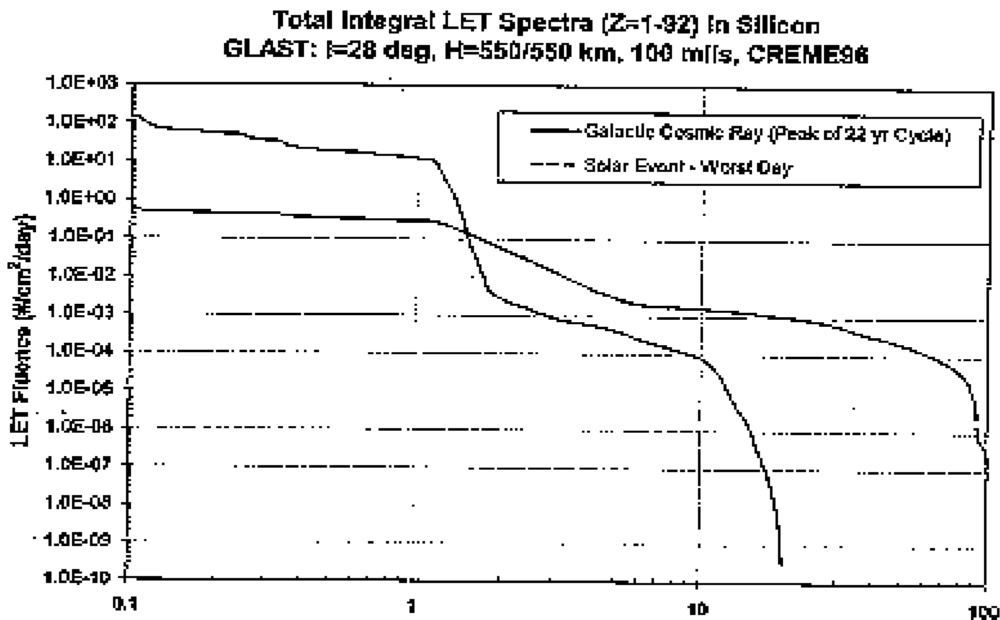


Figure 2. LET Spectra

Electronic parts shall be selected for tolerance to Single-Event Effects (SEE). A linear energy threshold of 8 MeV/mg/cm² (TBR) shall be used as a guideline to select parts for reasonably low probability (TBD) to Single-Event Upset (SEU) due to proton induced secondary. Electronic parts shall be selected for immunity to single event latch-up.

6.15 FAILURE ANALYSIS

GLAST LAT closed-loop system of failure documentation, analysis, and corrective action is a major contributor to reliability growth and continuous process improvement.

Reliability documentation and analysis of failure will be performed during acceptance test of components and the end-item. Failures below the component assembly acceptance test level and during integration efforts will be documented on nonconformance reports and analyzed by the MRB with appropriate reliability engineering support. All piece-part analysis will be performed. On flight software, analysis and reporting of failures and anomalies will start at the first integrated system test. A failure is defined as the inability of the end-item assembly to perform within the limits of its specified test requirement or specification.

The heart of our failure analysis and corrective action system is the MRB, which is chaired by the GLAST LAT Quality Assurance and PPE and is responsible for material review dispositions. The MRB also formulates and defines recommended actions for all failure analysis and corrective action activities. Subcontractors, vendors, or collaborators with acceptable MRB systems and personnel will be delegated MRB authority when appropriate for minor nonconformance. All nonconformance and failure reports will be stored in controlled files and will be made available for review.

6.16 PARTS CONTROL BOARD (PCB)

A parts control board (PCB) shall control the management, selection, and standardization of parts and materials used on GLAST LAT space flight instruments. The PCB members shall consist of representatives from the departments listed below. Signature requirements for PCB disposition are also listed below.

- Parts Engineering Representative – Chairman (signature required).
- Product Assurance Representative (signature required).
- Electrical Engineering or other designated technical representative (signature when required).
- NASA/GSFC Parts Organization Representative or designated alternate (signature when present).
- NASA/GSFC Materials Organization Representative or designated alternate (signature when required).
- Reliability Engineering Representative (signature not required)

The PCB shall be responsible for the generation and maintenance of a Program Approved Parts List (PAPL). The PCB shall be responsible for assuring every part on the PAPL meets the requirements of the program. The PCB shall also be responsible for the disposition of nonconforming parts, part problem resolution, and approval of all parts. The PCB chairman is responsible for publication of the PCB meeting minutes and submittal of those minutes to GSFC. The meeting minutes shall be submitted to GSFC within 3 working days of the PCB meeting. The PCB chairman is also responsible for documenting all approvals, disapproval’s, and other dispositions. Disposition cannot be made without securing signatures of the required PCB member signatories on the appropriate approval request forms (for a sample of the request form, see Appendix D). The requestor is responsible for providing the PCB with sufficient pertinent background information about the specific situation, such that each PCB signatory is assured acceptance of the nonconforming part does not form a significant reliability risk to the operation of the instruments over the life of the program. Approval of part screening and quality conformance inspection testing which does not meet the requirements specified in 311-INST-001 for quality level 2, shall require the concurrence of the PCB including the cognizant NASA/GSFC parts organization representative.

PCB meetings will be held when needed. GSFC participation at PCB meetings is not required, however, GSFC shall be notified, and invited to attend, at least 7 days in advance of upcoming meetings. For PCB items that require

immediate attention (production stoppages), 7 day advanced notification is not required, but an expeditious attempt to notify GSFC will be made. The meeting notice shall include a list of parts to be reviewed as a minimum. All parts falling into the categories listed in section 6.1 paragraphs 10 through 12 herein are to be reviewed by the PCB and shall be submitted for review/approval using a PCB submittal form.

The NASA/GSFC parts organization representative shall have voting rights at the meetings, and reserve the right to reverse any decisions of the PCB within 10 days after receipt of the PCB meeting minutes. Decisions not reversed within the 10 days shall be considered as concurred.

6.17 PART IDENTIFICATION LIST (PIL)

The GLAST LAT Project Approved Parts List (PAPL) will be the only source of approved parts for project flight hardware, and as such may contain parts not actually in flight design. Only parts that have been evaluated and approved by the PCB will be listed in the PAPL. Parts shall be approved for listing on the PAPL before initiation of procurement activity. The criteria for PAPL listing will be based on 311-INST-001 and as specified herein. The PCB will assure standardization and the maximum use of parts listed in the PAPL. The PAPL and all subsequent revisions will be available for GSFC review upon request. The final PAPL will be converted into the Parts Identification List (PIL), which will list all parts planned for use in flight hardware. An As-Built Parts Lists (ABPL) or final PIL will also be prepared and submitted to GSFC with information such as parts manufacturers and lot date code. A draft format of the PIL is attached (see Appendix E).

7 GUIDELINES FOR USE OF HIGH RELIABILITY INDUSTRIAL/COMMERCIAL PLASTIC ENCAPSULATED MICROCIRCUITS (PEMs)

7.1 SELECTION CRITERIA

Part Selection shall be dependent on the part manufacturer's test data, experience with the manufacturer, other OEM experience, or published test data. Selection shall be made on a part manufacturer and part number basis. It is noted that reliability test data is often technology or family based and may be different for various part types from the same manufacturer. Parts shall be selected based on part manufacturer or reliability test data, which may consist of qualification test data, reliability process monitor control test data, OEM reliability test data, or other OEM reliability test data. Combinations of test data from similar parts and the same packages may be used if acceptable to the PCB. Test data is obtained for each significant known failure mode and the failure rates added together to establish an overall failure rate metric.

Failure rate may be dependent on the operating temperature of the active area, such as the junction temperature of active components. It should be noted that the typical thermal resistance of Plastic Encapsulated Microelectronics is higher than that for their ceramic counterparts.

Heat conduction is usually through the package leads and many advanced packaging techniques such as copper lead frames and copper heat spreaders and thermal pipes are now being used to enhance the thermal conduction paths. New families of parts using advanced technology (e.g. highly integrated low power CMOS technology) so that thermal dissipation is often very low. The actual junction temperature is computed for each part.

The PPE should also review the methodology of the manufacturer's controls of manufacturing procedures and internal material selection. The actual procedures and internal material specifications are usually proprietary but should be reviewed to the extent they are available. Critical processes, as determined necessary, must be under Statistical Process Control.

Preference shall be given to parts from sources that would necessitate the least evaluation effort. In these circumstances preference shall be given to the following parts:

1. Parts manufactured by best-in-class suppliers, especially those with QML (http://www.dscc.dla.mil) production and heritage.
2. Parts manufactured on high volume standard production lines

3. Parts with the proven ability to operate reliably in extreme environments
4. Parts approved for other space programs (NASA, ESA, NASDA)

All parts that require further reliability assessment shall be submitted for PCB evaluation.

As a general rule, the PPE and PCB remains responsible for the selection of each part, taking into account the following:

5. Maximum use of previously approved parts with established reliability history.
6. Minimization and standardization of the number of different generic part types and families.
7. Taking possible obsolesce into account. Multiple sources preferred.
8. Application of de-rating requirements shall be verified by design assurance.
9. Tolerances to radiation exposure including total dose, latch up and single events for hybrids, microcircuits, transistors, and diodes.

PEM parts shall be selected to withstand all the environmental conditions specified for the project specified herein. Parts shall be selected on the basis of proven characterization/qualification from approved manufactures or sources employing effective Product Assurance Programs in manufacturing and test. When selecting items that have been previously approved, the PPE shall implement a characterization/qualification program to comply with the GLAST LAT requirements.

Evaluation of PEM should include the materials used in construction, fabrication (assembly and test) and quality control techniques. Data should be evaluated for case material, package type, lead finish, lead material, die technology, internal connection technologies (die attached to lead frame or terminals, die bonds and equipment, connection material interfaces), internal wire size and fragility assessment, and internal wiring process automation and controls were possible

High volume High Reliability Industrial Parts have greater process control and more automation than the lower volume parts (usually made in intermittent - start and stop - production) so that internal construction is more robust. In particular, Plastic Encapsulated Microcircuits have tight, automated fabrication procedures minimizing past concerns such as seal integrity, package ruggedness in high mechanical shock or random vibration environments, wire bond integrity, and internal conductive particle intermittent shorting.

7.2 PARTS RESTRICTIONS AND MOISTURE SENSITVITY

Use of PEMs shall be agreed on a case-by-case basis, during the PCB review/approval process. The part manufacturer shall initially qualify all parts/technologies and major process changes shall be requalified.

Moisture inside a PEM turns to steam and expands rapidly when the package is exposed to the high temperature of vapor phase reflow, infrared soldering, or if the package is submerged in molten solder or wave solder. Under certain conditions, the pressure from this expanding moisture can cause internal delaminating of the plastic from the chip and/or lead frame, internal cracks that do not extend to the outside of the package, bond damage, wire necking, bond lifting, thin film cracking, or cratering beneath the bonds. In the most severe case, the stress can result in external package cracks. This is commonly referred to as the “popcorn” phenomenon because the internal stress causes the package to bulge and often crack with an audible “pop”. Surface Mount Devices (SMDs) are more susceptible to this problem than the through-hole parts, because they are exposed to higher temperatures during reflow soldering. A reason for this phenomenon is that the soldering operation must occur on the same side of the boards as the SMD. For the through-hole parts, the soldering operation occurs under the board, which shields the parts form the chip or mount pad interface to the outside package surface, which has been identified as a critical factor in determining moisture sensitivity. Test method JESD22-A112, “Moisture-Induced Stress Sensitivity for Plastic Surface Mount Devices”, and JESD22 – A113, “Preconditioning of Plastic Surface Mount Devices”, will be used to assist in selecting and designing for PEMs applications. Inspections may include acoustic microscopy IAW JEDEC-STD-035, to help detect visually unseen, internal delaminating occurring as a result of “popcorning" conditions on sample pieces.

IPC/JEDEC J-STD-033, Standard for Handling, Packing, Shipping, and Use of Moisture/Reflow Sensitive Surface Mount Devices, describes the standardized levels of floor life exposure for moisture/reflow-sensitive SMDs. This

standard also includes handling, packing, and shipping requirements necessary to avoid moisture/reflow-related failures. These methods are provided to avoid damage from moisture absorption and exposure to solder reflow temperatures that can result in yield and reliability degradation. By using these procedures, safe and damage free reflow can be achieved, with dry packaging process, providing a minimum shelf life capability in sealed dry-bags of 12 months from the seal date.

JESD22-A113, Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing, is an industry standard preconditioning flow for nonhermetic SMDs that is representative of a typical industry multiple solder reflow operation. The semiconductor manufacturer should subject these SMDs to the appropriate preconditioning sequence of this test method prior to specific in-house qualification and reliability monitoring to evaluate long term reliability which might be affected by the solder reflow process such as convection, convection/IR, Infrared (IR), and Vapor Phase (VPR).

7.3 CLASSIFICATION OF REQUIREMENTS

The qualification, screening and QCI requirements for PEMs are delineated as follows:

- Manufacturer’s Capability Approval
- Qualification Basis
- Screening
- PEM Assembly Process
- Radiation Hardness Assurance (RHA)

7.3.1 MANUFACTURER’S CAPABILITY APPROVAL

Prior to procurement of PEMs intended for the use in GLAST LAT, the manufacturer’s capability to comply with the requirements of this document and the applicable device detailed drawing must be verified by the user. This applies for QML-38535 and non-QML suppliers.

7.3.1.1 QML Certified Manufacturer’s.

For devices manufactured by QML-38535 suppliers and produced on QML lines with QML approved process controls and technologies with plastic parts (which are not otherwise available through an established Standard Military Drawing (SMD)), additional certification is not required, but data should be reviewed for the intended application. When the SCD or procurement specification specifies part types or functions require different technologies or facilities from those used for the QML parts, a capability assessment shall be performed in accordance with MIL-PRF-38535.

7.3.1.2 Minimum Reliability for Qualification and Screening Requirements.

Data from a combination of qualification and reliability process monitor for the same die and the same package should be used where available. Equivalent testing under accelerated conditions such as higher temperature and time may be used provided it is validated using either the Arrhenius equation with validating test data for the Activation Energy or MIL-STD-883, Method 1005. Coffin-Manson equation may be used to accelerate the Temperature Cycling testing (using exponent of 4) and Peck Model may be used to accelerate the moisture corrosion testing of Autoclave or HAST to more severe test environments.

All parts to be incorporated into flight hardware shall be submitted to screening tests. The screening test requirements shall be designed so that accumulated stress will not jeopardize reliability. All performed screening shall be documented. All screening tests shall be performed at the parts manufacturer or at approved test houses.

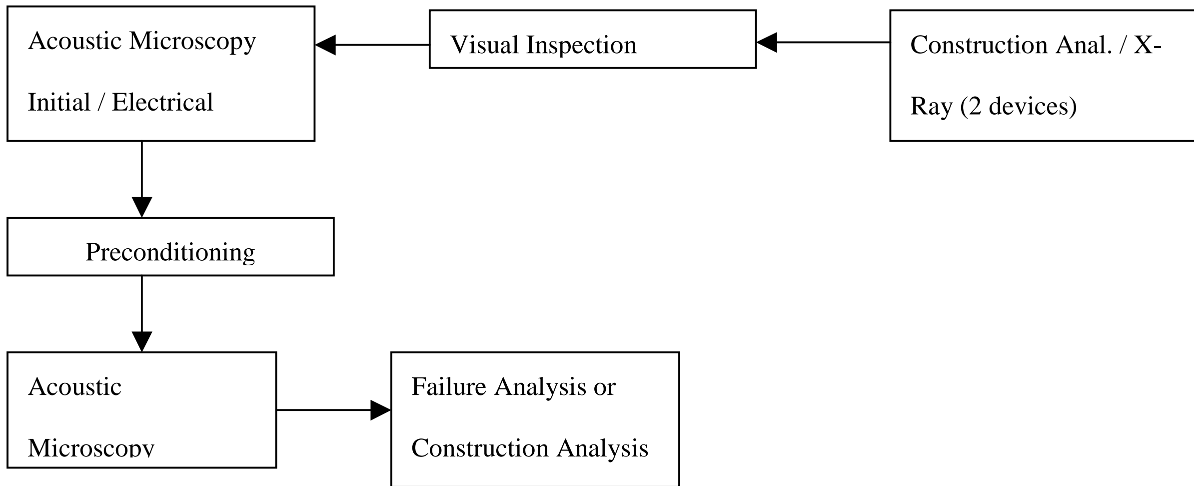
7.3.2 QUALIFICATION

The most effective qualification procedure is one, which can be used to estimate the reliability of a given part for a variety of different applications. Qualification shall be accomplished by history, similarity, existing test data, or by qualification testing for different part test levels.

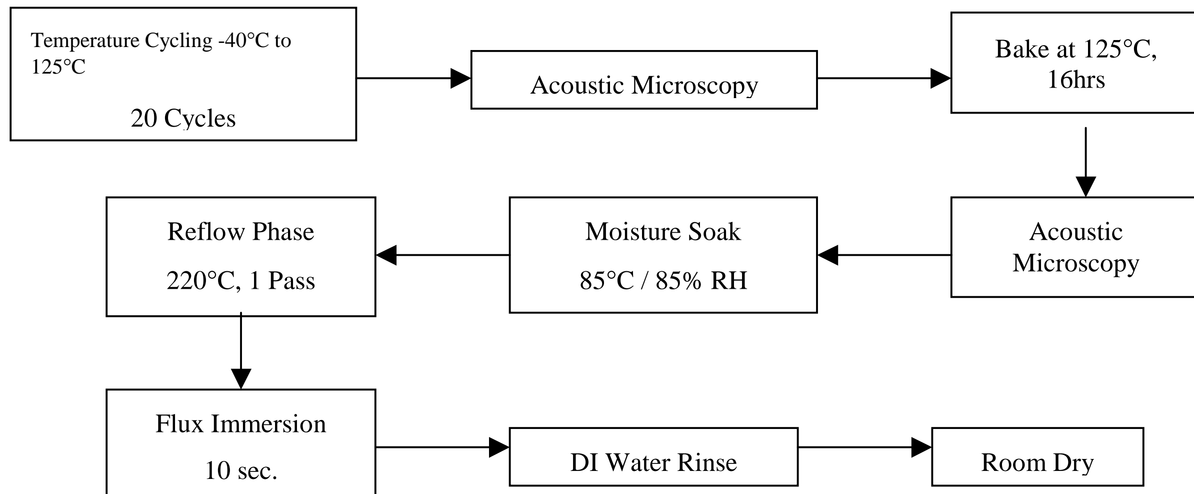
7.3.2.1 PEM Qualification Plan

This qualification process involves an incoming inspection, construction analysis, preconditioning sequence (to simulate storage and assembly).

TEST FLOW (PEMs)



PRECONDITIONG SEQUENCE
(Sample 5 pieces Max.)



7.3.2.2 Test Failure Criteria

Test failures are defined as devices not meeting the individual device specification, criteria specific to the test, or the specifications in the supplier's data sheet. Any device that shows external physical damage attributable to the environmental test is also considered a failed device. If the cause of failure is agreed to be due to mishandling or ESD, the failure shall be discounted, but reported as part of the data submission.

7.3.2.3 Screening

Defects in PEMs are often attributable to lack of control in material quality and manufacturing processes, and the presence of contamination. Besides product defects due to poor material quality, defects can be different from one manufacturer to another, and from one process to another.

Commercial parts normally do not receive 100% screening or lot acceptance tests as part of the standard flow, except for new products or high-density devices. Instead of 100% screening, suppliers generally use continuous process control and statistical methods to control quality. All PEMs procured to manufacturer's standard flow shall be screened in accordance with Table 1.

PPE is responsible for specifying device unique requirements not specified in Tables 1. The following MIL-STD-883 tests shall not be performed since epoxy molding protects the die and wire and the following devices do not have a cavity:

- Seal (Method#1014)
- Constant Acceleration (Method#2001)
- PIND (Method#2020)

7.4 Suppliers/Distributors

1. Commercial PEM suppliers have a tiered level of service tied to sales volume of individual customers; i.e., the bigger the buyer, the more attention you get. Smaller volume requirements are serviced through distributors and the level of support varies, depending on distributors. Most spacecraft builders are small volume buyers; hence, they will have to use distributors.
2. Distribution should be evaluated for ESD precaution, handling, storage and shipping. Distributors can play a vital role in after-sale service and in obtaining reliability information. Users can benefit in several ways by buying from distributors:
   - Cost effective for small volume buyers
   - Warranty and technical support

7.5 Packing and Storage Conditions

All PEMs shall be packed in dry-bag packing with desiccant, and special controlled storage conditions (moisture barrier bags). PEM parts shall be stored in a temperature controlled, clean, and dry environment, preferably dry nitrogen, and will be properly protected during test handling as well as all stages of manufacturing. Rebake and reseal in bags with fresh desiccant if necessary and always store in nitrogen cabinets after each use. Surface mount devices should be stored at Temperature < 30°C and Relative Humidity < 55%.

8 DESTRUCTIVE PHYSICAL ANALYSIS PROCEDURE FOR PEMS

8.1 External Visual Examination.

Inspect each sample at 3X to 10X magnification. One photograph of one typical device showing all marking shall be taken. Failure criteria of MIL-STD-883D, Method 2009, "External visual" are applicable except paragraphs 3.3.1.b, 3.3.2.a, 3.3.3, 3.3.4, 3.3.5.e, 3.3.5.g, 3.3.6.b, 3.3.7, and 3.3.8. Additionally, look for the following defects:

- Package nonplanarity, warping, or bowing,
- Foreign inclusions in the package, voids and cracks in the plastic encapsulant
- Deformed leads.

8.2 X-ray Examination

The purpose of this examination is to find the die and wire placement for future decapsulation and to detect internal defects of the package. Look for the following defects:

- Foreign objects, voids, and filler conglomerates in the encapsulant,
- Voids in the die attach material,
- Misaligned leads,
- Burrs on lead frame (inside the package),
- Poor wire bond geometry (wires that deviate from a straight line from bond to external lead or have no arc and make a straight line run from die bonding pad to lead),
- Swept or broken wires,
- Improper die placement.

Radiographs shall be taken of sample device in two views 90 degrees apart (top and side views). MIL-STD-883D, Method 2012, “Radiography” is applicable.

8.3 Acoustic Microscopy

Samples shall be subjected to the acoustic micro imaging analysis. The purpose of this examination is to nondestructively detect the following defects:

- Delamination of the molding compound from the lead frame, die, or paddle;
- Voids and cracks in molding compound;
- Unbonded regions and voids in the die-attach material (if possible).

The apparatus and materials for this test shall include:

1. Ultrasonic imaging equipment based on reflection (pulse echo) technology in which a single focused acoustic lens mechanically scans a tiny dot of ultrasound (in frequency range of 10 to 150 MHz) through the sample. A reflection is generated at each interface and returned to the sending transducer for processing and image generating. Signal processing shall allow information to be gathered from multiple levels within the sample. A C-Mode Scanning Acoustic Microscope (C-SAM) can be used for this purpose.
2. Deionized water shall be used as a medium fluid to provide acoustic coupling between the sample and the transducer.

8.3.1 Examination Sites

Examination of the package for voids, cracks, and delaminations shall be performed on each sample at six areas:

1. Interface between the die and molding compound;
2. Interface between the lead frame and molding compound (top view);
3. Interface between the paddle periphery and molding compound (top view);
4. Die-to-paddle attachment interface (if possible);
5. Interface between the paddle and molding compound (back view);

6. Interface between the lead frame and molding compound (back view).

NOTE

- Combined C-mode scans can be performed to investigate more than one area during one scanning run.
- Die-attach inspection shall be performed per MIL-STD 883D, Method 2030, "Ultrasonic inspection of die attach" for the parts with the die mounted onto a substrate or heat sink. This standard can also be applicable for other package types provided the resolution is adequate to detect voids in the attachment material.

PROCEDURE

Package surface roughness, mold marks, labels and surface defects create additional ultrasonic wave reflections and hinder analysis results. Packages with nonflat shapes may require milling or grinding before analysis.

- Remove labels from the area to be scanned. Note all mold marks or defects, which may have affected the scan results. Flatten the surface using a grinding/polishing and wet the surface with alcohol if necessary.
- Place sample in the holder in deionized water with the upper surface parallel to the scanning plane of the acoustic transducer. Sweep air bubbles away from the unit surface and from the bottom of the transducer head.
- Set the focus by maximizing the amplitude of the reflection from the die-molding compound interface and perform acoustic scanning.
- If the lead frame-molding compound interface was not in focus, reset the focus and perform scanning of this interface.
- Refocus the transducer to the periphery of the paddle-molding compound interface and perform acoustic scanning.
- Refocus the transducer to the die attachment (if possible) and perform acoustic scanning. If the image is not sharp enough, try to view the area from the backside of the part.
- Turn the part over, sweep air bubbles away from the unit, focus the transducer to the backside of the die paddle, and perform acoustic scanning.
- Refocus the transducer to the lead frame-molding compound interface and perform acoustic scanning.

8.3.2 Evaluation criteria

In the device examination, the following aspects shall be considered as unacceptable and devices, which exhibit any of the following defects, shall be rejected:

1. Cracks in plastic package intersecting bond wires.
2. Internal cracks extending from any lead finger to any other internal feature (lead finger, chip, die attach paddle) if crack length is more than a half of the corresponding distance.
3. Any crack in the package breaking the surface.
4. Any void in molding compound crossing wire bond.
5. Any measurable amount of delamination between plastic and die.
6. Delamination of more than half of the backside or top peripheral area of the interface between the paddle and plastic.
7. Complete leadfinger delamination from the plastic (either top or backside).
8. Delamination of the top tie bar area for more than half of its length.

NOTE

If rejectable internal cracks or delaminations are suspected, a polished cross section may be required to verify the suspected site.

8.4 Die Penetrant/Cross-Sectioning Test.

Two devices, or 40% of the DPA samples, whichever is larger, shall be subjected to this examination. The purposes of this test are as follows:

- To inspect wire bonding (to the die and lead frame);
- To examine die attachment for voiding and cracks;
- To characterize integrity of molding compound;
- To ensure that there is no direct way (along the leads) for moisture and contamination to reach the die.

8.4.1 Procedure

Die penetrant test shall be performed per MIL-STD-883D, Method 1034, with the following deviations:

1. Any appropriate microscope with ultraviolet illumination can be used.
2. All samples shall be examined under ultraviolet illumination after the die penetrant hardening before cross sectioning using low power microscope (10X - 40X). Look for external cracks in sites other than the lead-plastic interface where some separation between the lead and the package is possible.
3. Half of the samples shall be sectioned along one side and half along the other side of the package in three planes (minimum). The planes shall cross the package along the leads (approximately in the middle) in vicinity of the paddle edge, approximately in the middle of the die, and in vicinity of the other paddle edge. Parts with the paddle tie bars shall be sectioned along the bars. At least three planes shall cross the wire bond to the die and to the lead. If suitable, a sample can be sectioned into two parts before potting.

8.4.2 Evaluation Criteria

The following defects shall be rejected.

1. Package cracks and delaminations;
   - Any evidence of die penetration to the die or the paddle;
   - Any evidence of external cracks other than between the lead and plastic;
   - Any evidence of die penetration of more than 2/3 of the lead length;
   - Any evidence of die penetration of more than half of the tie bar length.
2. Bonding:
   - Lifted and shifted bonds;
   - Intermetallic compound formation in areas of reliability concern.
3. Die attach: voiding of more than 50%.
4. Molding compound:
   - Foreign intrusions;
   - Voids in vicinity of bonding wires.

8.5 Decapsulation

The purpose of this section is to provide guidelines for possible decapsulation methods for failure analysis (FA) and destructive physical analysis (DPA) of plastic encapsulated semiconductor devices. It is also intended to characterize advantages and disadvantages, and indicate possible pitfalls.

8.5.1 Preliminary Steps

X-ray analysis should be performed before decapsulation to learn die shape, placement and size; and to determine the height of the bond wires. This information will assist in choosing the correct mask or gasket and/or depth of the trench to be milled in the package surface.

The samples should be baked before wet decapsulation. This step is intended to remove all moisture from the package so that damage will not occur due to acidic corrosion of the metallization.

CAUTIONS

- Results of subsequent examinations depend heavily on decapsulation quality. Detailed records about decapsulation process irregularities and possible artifacts should be maintained.
- Do not expose wire bonds at the lead frame when using wet etching techniques. These bonds are frequently made to silver plated areas and chemical etchants will quickly degrade them.

8.5.2 Milling

This step is not necessary but is often useful for Manual Wet etching and Plasma etching. Milling prevents the leads from breaking off by ensuring that the chip surface is exposed before the lead frame, and reduces the time required for etching.

Any suitable milling machine is acceptable; use of a dental drill to create a small impression is possible but not preferable because a flat surface would not result. The procedure is as follows:

1. Using X-ray data, calculate the depth of the trench to be milled.
2. Install the part into the fixture of a milling machine. The surface being worked should be parallel with the milling plane.
3. Start milling, moving the mill tip down to the calculated depth. Mill the trench slightly longer and wider than the die.

To ensure that the bond wires remain intact during milling, it is recommended that approximately 0.2 mm of plastic be allowed to remain covering them.

8.5.3 Suggested Techniques

8.5.3.1 Manual Wet Etching

Advantage: A quick result is possible with readily available equipment. Disadvantage: Removal of contamination from the surface of the die preventing chemical analysis; the method requires very careful attention to safety.

Apparatus and materials

- Heating plate, metal block, beaker, aluminum weighing dish, and disposable dropper.
- Red fuming nitric or sulfuric acid can be used as etchants. Acetone, isopropanol, or methanol can be used for rinsing.

Notices

- Red fuming nitric acid can be used in most cases. Sulfuric acid can be used as a solvent specific to anhydride epoxies.

- Red fuming nitric acid has little effect on plastic at room temperature, but elevating the temperature to approximately 100°C will cause it to decapsulate a device in few minutes. Higher temperatures will only decompose the acid. When heated in an open beaker, the acid will evaporate NO_2 and absorb moisture with time, thus becoming diluted and converted into yellow nitric acid. Dilute (yellow) nitric acid is not suitable for decapsulation purposes because it reacts with the metal in the devices.
- To have an effect on epoxy, sulfuric acid must be heated to about 150°C. Use deionized water for rinsing.

Procedure

1. Mill a trench or create a small impression, according to section 7.5.2.
2. Make a mask using aluminum foil adhesive tape shielding the specific areas not to be etched.
3. Install the part on a metal (copper or aluminum) block to provide heat directly to the bottom of the device. Then place it in an aluminum-weighing dish on a plate heated to approximately 90°C and wait several minutes to allow the package to heat up.
4. Pour a small quantity of red fuming nitric acid into a beaker and apply several drops to the device with the dropper.
5. Cleanup: rinse with cold nitric acid for a few seconds, rinse in a spray of acetone, then in isopropanol or ultrasonically clean in methanol. Blow with dry air.
6. Repeat steps 3-5 until the die is exposed.
7. If necessary, perform a plasma cleanup with a 10:1 mixture of 0_2:CF_4 in a barrel plasma (50W, 30-60 min.).

Cautions

- It is very important to keep the part hot and the exposure time very short for reaction with acid.
- There are safety hazards with this process. All safety procedures should be invoked.

Table 1. Screening Requirements for PEM Integrated Circuits

Inspection/Test	Methods/Conditions	Test quality level 2/Grade B		
		Q/Class N	HI-REL	Commercial
1. Acoustic Microscopy (100%)	section 6.3 herein	✓	✓	✓
2. DPA 1/	section 6.0 herein.	✓	✓	✓
3. Temperature Cycling 2/	MIL-STD-883, TM1010 /B	✓	✓	✓
4. Initial Electrical Measurements	per applicable device specification	✓ Read only	✓ Read only	✓ Read only
5. Burn-in 3/	per applicable device specification Duration (hours)	✓ 72/160	✓ 72/160	✓ 72/160
6. Final Electrical Measurements 4/	per Table 3 herein and applicable device specification	✓ Read only	✓ Read only	✓ Read only
7. Calculate PDA 5/		5%	5%	5%
8. External Visual	MIL-STD-883, TM2009 / and 6.1	✓	✓	✓

1/If parts fail DPA, consult with parts engineer for the lot may have to be rejected or additional screens imposed.

2/Cycle between maximum and minimum storage temperature of device for 10 cycles, no power applied during test.

3/See the burn-in duration is indicated as "Static/Dynamic". For example, burn-in duration 72/160 requires 72 hours of static burn-in (if applicable) and 160 hours of dynamic burn-in (if applicable). S-311-INST-001 specifies an ambient of 125 °C. This temperature shall only be used if the manufacturers specified max. Junction temperature for the plastic device is not violated. Otherwise, choose a temperature commensurate with the max. Junction temperature taking into account joule heating for device under test. The duration hours at a lower burn-in temperature must be extended to yield equivalent hours duration at 125 °C. These calculations generally require activation energy for the Arrhenius equation associated with specific failure mechanisms.

4/For field programmable (nonerasable) devices, such as fuse-linked PROMS, PALs and anti-fuse base FPGAs, step 5 shall be performed after the programming, even if they were performed earlier on the blank devices.

5/PDA applies to cumulative failures during all burn-in steps. PDA applies to the functional failures.

APPENDIX A

DERATING GUIDELINES
FOR
HERMETIC DEVICES

(for more details, refer to the PPL-21 web-site http://nepp.nasa.gov)

Capacitors

Voltage derating is accomplished by multiplying the maximum operating voltage by the appropriate derating factor appearing in the table below.

Type	Military Style	Voltage Derating Factor	Maximum Ambient Temperature
Ceramic	CCR. CKS, CKR, CDR, DSCC-DWG-87106, PS	0.6	110ºC
Glass	CYR	0.5	110ºC
Plastic Film	CRH, CHS	0.6	85ºC
Tantalum, Foil	CLR25, CLR27, CLR35, CLR37	0.5	70ºC
Tantalum, Wet Slug	CLR79, CLR81, CLR90, CLR91	0.6 0.4	70ºC 110ºC
Tantalum, Solid	CSR, CSS, CWR	0.5 0.3	70ºC 110ºC

Circuit Breakers

Circuit breaker contacts are derated by multiplying the maximum rated contact current (resistive) by the appropriate contact-derating factor listed below.

Contact Application	Contact Current Derating Factor	Maximum Ambient Temperature
Resistive	0.75	20ºC below maximum rated temperature
Capacitive	0.75	
Inductor	0.40	
Motor	0.20	
Filament	0.10	

Fuses

Fuses are derated by multiplying the rated amperes by the appropriate derating factor listed below.

Fuse Current Rating (Amperes) @ 25ºC	Current Derating Factor	Derated Fuse Current (A)	Temperature Derating Factor	Remarks
2 – 15	50%	1 – 7.5	Apply additional derating of 0.5%/ºC for an increase in the temperature of fuse body is above 25ºC	
1, 1 ½	45%	0.45, 0.675		
¾	40%	0.3		
½	40%	0.2		The flight use of fuses rated ½ A or less requires application approval by the parts specialist and/or project office
3/8	35%	0.13125		
¼	30%	0.075		
1/8	25%	0.03125		

Connectors

Connectors of all types/styles are derated by limiting the temperature seen by the dielectric insert due to ambient temperature and the effects of resistive heating.

Operating Voltage Derating	25% of the rated dielectric withstanding voltage at sea level
Temperature Derating of the Dielectric Insert	Temp. Rating ≥ Ta + Toh + 50ºC

Notes: Ta = Ambient Temperature, Toh = Ohmic Heating Temperature

Crystals:

Rated Drive Level	50% of the rated value.
Operating Temperature	10ºC higher than the minimum specified value
	10ºC lower than the maximum specified value
Frequency Shift	Allow for 4 times the frequency shift in the procurement specifications

Crystal Oscillators:

Crystal oscillators are hybrid parts that contain a number of microcircuits and other electronic components. Crystal oscillators should be derated at the individual component level. Crystal current should be derated to 50% of the rated value. In cases where start-up time is critical, 75% of the rated value should be used. Some of the components used in the crystal oscillator may degrade in radiation environment. The crystal oscillator parameters that may get affected include current, frequency and frequency shift. Consult the project radiation specialist to evaluate the effect of radiation environment on the individual components and hence on the crystal oscillator.

Filters

Derating is accomplished by multiplying the current and voltage by the appropriate derating factor appearing in the chart below.

Class	Stress Parameter (Note 1)	Derating Factor
ALL	Rated Current	0.50
	Rated Voltage	0.50
	Maximum Ambient Temperature	85ºC, or 30ºC less than maximum rated temperature, whichever is less

Note 1: Applies to rated operating current or wattage, not the absolute maximum

Inductors and Coils

Inductors are derated by reducing the maximum operating temperature based on the insulation class used and reducing the operating voltage. See notes below.

<table>
<tr><th colspan="2">Insulation Class</th><th colspan="3">Maximum Operating Parameters</th></tr>
<tr><td>MIL-PRF-39010</td><td>MIL-PRF-15305</td><td>Rated Operating Temperature</td><td>Derated Operating Temperature</td><td>Operating Voltage</td></tr>
<tr><td>-</td><td>O</td><td>+85°C</td><td>+65°C</td><td rowspan="4">Derate to 50% of the rated dielectric withstanding voltage</td></tr>
<tr><td>A</td><td>A</td><td>+105°C</td><td>+85°C</td></tr>
<tr><td>B</td><td>B</td><td>+125°C</td><td>105°C</td></tr>
<tr><td>F</td><td>-</td><td>+150°C</td><td>130°C</td></tr>
</table>

Notes:

1. Maximum operating temperature equals ambient temperature plus temperature rise, plus 10°C (allowance for hot spot). Compute temperature rises as follows:

   Temperature rise test (per MIL-T-27, 4.8.12)

   Temp. Rise (°C) = (R - r)/r x (t + 234.5°C) – (T – t)

   - R = winding resistance at elevated temperature
   - r = winding resistance at ambient temperature
   - t = specified initial ambient temperature (°C)
   - T = maximum ambient temperature (°C) at time of power shutoff.

   T should not differ from t by more than 5°C.

2. The insulation classes of MIL-style inductive parts generally have maximum operating temperature rating based on a life expectancy of 10,000 hours. The maximum operating temperatures in this table are selected to extend the life expectancy to 50,000 hours.

3. Custom made inductive devices should be evaluated on a materials basis to determine the maximum operating temperature. Devices with temperature ratings different from the military insulation classes should be derated to 0.75 times maximum operating temperature.

Relays

Subtable T (Ambient Operating Temperature)		Subtable R (Cycle Rate)		Subtable L (Load)	
Temperature Range	Factor	Cycle Rate per Hour	Factor	Load Application	Factor
+85ºC to +125ºC	0.7	>10	0.85	Make, break and/or carry loads with an on-time duration of 0 to 500ms. Off time is equal to or greater than n time.	1
+40ºC to +84ºC	0.85	1 to 10	0.90	Carry-only loads. Relay does not make or break the load. Maximum on time is 5 minutes. Off time is equal to or greater than on time.	1.5
-20ºC to +39ºC	0.9	<1	0.85	All other load conditions	0.8
-65ºC to -21ºC	0.85				

Notes:

1. DO NOT derate coil voltage or current. Operating a relay at less than nominal coil rating can result in either switching failures or increased switching times. The latter condition induces contact damage because of the longer arcing time, thus reducing relay capacity.
2. For additional information see PPL-21.

Resistors

Style	Description	Derating Factors (1)	Derating Factors (2)	Derating Temperatures		Specification Maximum Storage Temperature
		Power	Voltage	T1	T2	T3
G311P672	Fixed, High Voltage	0.6	0.8	70	94	110
G311P683	Fixed, Precision, High Voltage	0.6	0.8	125	185	225
G311P742	Fixed, Low TC, Precision	0.6	0.8	125	155	175
RBR	Fixed, Wirewound (accurate), Established Reliability					
1%		0.6	0.8	125	137	145
0.5%		0.35	0.8	125	132	145
0.1%		0.25	0.8	125	130	145
RWR	Fixed, Wirewound (power type), Established Reliability	0.6	0.8	25	160	250
RCR (3)	Fixed, Composition (Insulated), Established Reliability	0.6	0.8	70	(4)	(4)
RER	Fixed, Wirewound (power type), chassis mounted, Established Reliability	0.6	0.8	25	160	250
RTR	Variable, Wirewound (lead screw actuated), Established Reliability	0.6	0.8	85	124	150
RLR	Fixed, Film (insulated), Established Reliability					
100ppm		0.6	0.8	70	118	150
350ppm		0.6	0.8	70	103	125
RNC, RNR, RNN	Fixed, Film, Established Reliability	0.6	0.8	125	155	175
RM	Fixed, Film, Chip, Established Reliability	0.6	0.8	70	118	150
RZ	Fixed, Film, Networks	0.6	0.8	70	103	125
Others	Various	0.5	0.8	(5)	(5)	(5)

Notes:

1. For the ambient temperatures ≤T1, compute the resistor's derated power level by multiplying its nominal power rating by the appropriate derating factor. If the resistor is operated above T1, derate linearly from the T1 power level to the zero power level at T2. Exposing the resistor to temperatures exceeding T3,

even under no load conditions, may result in permanent degradation. The graphs that follow visually depict the power derating profiles described in tabular form above for the various resistor styles.

2. The maximum applied voltage should not exceed the lesser of the following: (1) 80% of the specified maximum voltage rating or (2) the square root of: the derated power (Watts) multiplied by the resistance of that portion of the element actually active in the circuit.

   This voltage derating applies to dc and regular ac waveform applications. For pulse and other irregular waveform applications, consult MIL-HDBK-978 or the manufacturer.

3. The last known source for military grade, carbon composition resistors ceased production in 1996. Derating guidelines are provided for projects using residual stock. NASA Parts Advisory NA-033 dated July3, 1996 discusses this diminishing source topic in detail. Consult the EPMIS (http://misspiggy.gsfc.nasa.gov) database for details of this advisory.

4. Determine the maximum storage temperature (T3) from the applicable detail specification. Compute the derated zero power temperature (T2) from the following formula:

   T2 = D(T3 – T1) + T1, where:

   T2 = Derated zero power temperature

   D = Derating Factor

   T3 = Maximum storage temperature from applicable specification sheet

   T1 = Rated power temperature.

5. Determine the rated power, the rated power temperature (T1), and the maximum storage temperature (T3) from the manufacturer's specification. Calculate the derated zero power temperature (T2) as per the previous note.

Thermistors

Positive Temperature Coefficient (PTC) thermistors are generally operated in the self-heat mode. Derate to 50 percent of the rated power, or as required by the detail specification.

Negative Temperature Coefficient (NTC) thermistors operated in the self-heat mode should be derated in accordance with the figure provided in PPL-21. Such parts should be derated to a power level causing maximum increase of 50 times the dissipation constant, or a maximum part temperature of 100°C, whichever is less.

Transformers

Transformers are derated by limiting the maximum operating temperature based on the insulation class used, and limiting the rated operating voltage to 50% of its maximum.

Insulation Class		**Derated Maximum Operating Parameters**	
MIL-PRF-27	MIL-PRF-21038	Temperature	Dielectric Withstanding Voltage
Q(+85ºC)	Q(+85ºC)	+65ºC	50% of maximum rated operating voltage
R(+1055ºC)	R(+105ºC)	+85ºC	
S(+130ºC)	S(+130ºC)	105ºC	
V(+155ºC)	T(+155ºC)	130ºC	
T(+170ºC)	U(+170ºC)	155ºC	

Notes:

1. Maximum operating temperature equals ambient temperature plus temperature rise, plus 10ºC (allowance for hot spot). Compute temperature rises as follows:

   Temperature rise test (per MIL-T-27, 4.8.12)

   Temp. Rise (ºC) = (R - r)/r x (t + 234.5ºC) – (T – t)
   - R = winding resistance at elevated temperature
   - r = winding resistance at ambient temperature
   - t = specified initial ambient temperature (ºC)
   - T = maximum ambient temperature (ºC) at time of power shutoff.

   T should not differ from t by more than 5ºC.

2. The insulation classes of MIL-style inductive parts generally have maximum operating temperature rating based on a life expectancy of 10,000 hours. The maximum operating temperatures in this table are selected to extend the life expectancy to 50,000 hours.
3. Custom made inductive devices should be evaluated on a materials basis and stressed at levels below the maximum operating temperature for the materials used. Devices having maximum rated operating temperatures in the range from +85°C to +130°C, should be derated as follows: maximum operating temperature (°C) equals 0.75 times maximum rated operating temperature. For devices with maximum rated temperatures outside this temperature range, consult the project parts engineer for temperature derating recommendations.

Wire and Cable

Wire Size (AWG)	Derated Current (Amperes)	
	Single Wire	Bundled Wire or Cable
30	1.3	0.7
28	1.8	1.0
26	2.5	1.4
24	3.3	2.0
22	4.5	2.5
20	6.5	3.7
18	9.2	5.0
16	13.0	6.5
14	19.0	8.5
12	25.0	11.5
10	33.0	16.5
8	44.0	23.0
6	60.0	30.0
4	81.0	40.0
2	108.0	50.0
0	147.0	75.0
00	169.0	87.5

Notes:

1. Derated current ratings are based on an ambient temperature of 70°C or less in a hard vacuum of 10^-6 torr.
2. The derated current ratings are for 200°C rated wire, such as Teflon™ insulated (Type PTFE) wire, in a hard vacuum of 10^-6 torr.
   a. For 150°C wires, use 80% of the value shown above.
   b. For 135°C wires, use 70% of the value shown above.
   c. For 105°C wires, use 50% of the value shown above.
3. The current rating for bundles or cables are base on bundles of 15 or more wires. For additional information see PPL-21.

Diodes

Derating is accomplished by multiplying the critical stress parameter by the appropriate derating factor in the chart below:

Diode Type	Critical Stress Parameter	Derating	Maximum Junction Temperature
General Purpose, Rectifier, Switching, Pin/Schottky, and Thyristors	Peak Inverse Voltage	0.70	125°C, or 40°C below the manufacturer's Maximum rating, whichever is lower
	Surge Current	0.50	
	Forward Current	0.50	
Varactor	Power	0.50	
	Reverse Voltage	0.75	
	Forward Current	0.75	
Voltage Regulator	Power	0.50	
	Zener Current	0.5(I-max + I-nom)	
Voltage Reference	Zener Current	N/A (1)	
Zener Voltage Regulator	Power Dissipation	0.50	
Bi-directional Voltage Suppressor	Power Dissipation	0.50	
FET Current Regulator	Peak Operating Voltage	0.80	
Microwave Diodes	Power Dissipation	0.50	
	Reverse Voltage	0.75	

Note:

Operate at the manufacturers specified Zener current to optimize temperature compensation. For additional information see PPL-21.

Transistors

Derating of transistors is accomplished by multiplying the appropriate stress parameter by its derating factor. Junction temperature must also be calculated and maintained below 125°C or 40°C below the manufacturer's maximum rating, whichever is lower.

Transistor Type	Critical Stress Parameter	Derating Factor	Maximum Junction/Channel Temperature
BIPOLAR General purpose, switching, and power	Power Current Voltage	0.50 0.75 0.75 (1)	125°C, or 40°C below the manufacturer's Maximum rating, whichever is lower
FIELD EFFECT JFET	Power Current Voltage	0.50 0.75 0.75 (1)	
MOSFET (2)	Power Current Voltage (V-ds) Voltage (V-fgs)	0.50 0.75 0.75 (1) 0.60 (1)	
RF/MICROWAVE Silicon GaAs	Power Current Voltage	0.50 0.75 0.75 (1)	

Notes:

1. Worst-case combination of DC, AC, and transient voltages should be no greater than the derated limit.
2. Power MOSFET devices under certain conditions are very susceptible to catastrophic failure mechanisms, specifically Single Event Burnout (SEB) and Single Event Gate Rupture (SEGR), resulting from heavy ion impact. It may be necessary to derate the drain to source voltage (V-ds) and gate to source voltage (V-gs) to 30 – 50 % og the maximum, depending upon the device type, the manufacturer, etc. Consult the applicable parts/radiation specialist for further information and applicable derating guidelines.

3. For additional information see PPL-21.

Digital Microcircuits

Derating of digital microcircuits is accomplished by multiplying the parameter by the appropriate derating factor in the chart below:

Critical Stress Parameters	**Bipolar Logic**	**CMOS Logic**		**Line Drivers/ Receivers**	**LSI/VLSI**		**ASIC - Digital and Mixed Signal**
		4000 A/B	**Other (3)**		**Biploar**	**CMOS**	
Absolute Maximum Supply Voltage (1)	(2)	0.70	0.80	0.75	(2)	(2)	(2)
Input Voltage	Under no circumstances should input voltage be allowed to exceed the supply voltage. Logic noise-margin levels should be derated by a factor of 0.80.						
Open Collector/Drain DC Output Voltage	0.80	0.80	0.80	0.80	0.80	0.80	0.80
Operating AC/DC Output Current or Fanout	0.80	0.80	0.80	0.80	0.80	0.80	0.80
Power Dissipation	0.75	0.75	0.75	0.75	0.75	0.75	0.75
Maximum Junction Temperature	100°C, or 40°C below the manufacturer's Maximum rating, whichever is lower						

Notes:

1. For those technologies where no supply voltage derating is specified, in no case shall the device maximum operating supply voltage be exceeded.
2. Use Manufacturer's recommended operating voltages.
3. Includes high speed (HCS/HCTS) and advanced (ACS/ACTS/AC/ACT)

Further derating may be required for radiation induced degradation. Consult the project radiation specialist for derating guidelines which account for radiation induced degradation in parts over the lifetime of each mission.

Linear Microcircuits

Derating of linear microcircuits is accomplished by multiplying the parameter by the appropriate derating factor in the chart below:

Critical Stress Parameter	Comparators	Sense Amplifiers	Operational / Differential Amplifiers	Other Amplifiers (1)	Voltage Regulators	Analog Switches	A/D and D/A Converters
Absolute Maximum Supply Voltage (2)	0.80	0.80	0.80	0.80		0.80	0.80
Differential Input Voltage (4)	0.70	0.70	0.70	0.70			
Single-Ended DC Input Voltage (4)					0.80	0.80	0.80
Open Collector/Drain DC Output Voltage	0.75	0.75					
Operating AC or DC Output Current	0.80	0.80	0.80	0.80	0.80	0.80	0.80
Maximum Short Circuit Output Current	0.80	0.80	0.80	0.80	0.80		
Power Dissipation	0.75	0.75	0.75	0.75	0.75	0.75	0.75
Maximum Junction Temperature	100°C, or 40°C below the manufacturer's Maximum rating, whichever is lower						

Notes:

1. Other amplifiers include current, voltage follower, instrumentation, video and sample and hold.
2. For devices with maximum ratings greater than 10V, derate by at least 2 V below the absolute maximum voltage rating of each rail.
3. V-in – V-out should be derated to 0.80.
4. Under no circumstances should the input voltage be allowed to exceed the supply voltage.

Further derating may be required for radiation induced degradation. Consult the project radiation specialist for derating guidelines which account for radiation induced degradation in parts over the lifetime of each mission.

Optoelectronic Devices

Derating of transistors is accomplished by multiplying the appropriate stress parameter by its derating factor. Junction temperature must also be calculated and maintained below 100°C or 40°C below the manufacturer's maximum rating, whichever is lower.

Device Type	Critical Stress Parameter	Derating Factor	Maximum Junction/Channel Temperature
Light Emitting Diodes	Power	0.50	Maximum junction temperature should be limited to 100°C or 40°C below the manufacturer's maximum rating, whichever is lower.
	Current	0.75	
	Voltage	0.75	
Photo Diodes	Power	0.50	
Photo Transistors	Current	0.75	
	Voltage	0.75	
Optocouplers	Power	0.50	
(1) (2)	Current	0.75	
	Voltage	0.75	

Notes:

1. For optimum coupling efficiency, use manufacturers recommended operating conditions.
2. Recent experiences have indicated that optocouplers, in general, are usually sensitive to Single-Event transients. Consult with an appropriate specialist prior to selecting optocouplers for flight applications.

Hybrids and Multi Chip Modules (MCMs)

Hybrids make an integral use of chips and discrete parts on a common substrate in a single package to meet the need for unique circuit requirements, often available as an individual microcircuits. On the other hand, the MCM is a chip-only technology with the substrate being an integral part of the product design, not simply a component carrier. The dice are mounted on or embedded in a multilayered substrate that is contained in a protective case that may be hermetic sealed or plastic encapsulated.

Normally the hybrid and MCM packages provide an inherent space saving advantage, however, there are some potentially adverse effects of high-density packaging:

a) Tight/close physical proximity – reduces isolation reduction, resulting in cross-talk
b) Concentrated areas of power dissipation – makes cooling more difficult, effecting reliability and performance.
c) Dissimilar adjacent materials/metals – reduces reliability under temperature extremes (TCE problems) and increases corrosion possibilities.

The failure mechanisms found in microcircuits and passive components, from electrical aging, electrical and mechanical wear out, and radiation, are also found in Hybrids and MCMs. Also, the Hybrid/MCM parts package has a significant effect on the part's life. Packages that dissipate heat effectively and/or protect the internal circuitry from the environment last longer.

APPENDIX B

DERATING GUIDELINES FOR PEM MICROCIRCUITS

Type			Environment	
Digital	**Package**	**Derating Parameter**	**Protected**	**Normal**
MOS	Plastic 1/	Supply Voltage	/3	/3
		Frequency	90%	80%
		Output Current	90%	80%
		Fanout	100%	90%
		Junction Temperature	90°C	85°C
	Plastic 2/	Supply Voltage	/3	
		Frequency	80%	
		Output Current	70%	
		Fanout	80%	
		Junction Temperature	70°C	
Bipolar	Plastic 1/	Supply Voltage	/3	/3
		Frequency	100%	90%
		Output Current	90%	80%
		Fanout	90%	80%
		Junction Temperature	90°C	85°C
	Plastic 2/	Supply Voltage	/3	
		Frequency	75%	
		Output Current	70%	
		Fanout	70%	
		Junction Temperature	70°C	

Table 1. Digital MOS and Bipolar Microcircuit Derating Guidelines

Type			Environment	
Digital	Package	Derating Parameter	Protected	Normal
MOS	Plastic 1/	Supply Voltage	/3	/3
		Input Voltage	80%	70%
		Frequency	90%	80%
		Output Current	90%	80%
		Fanout	100%	90%
		Junction Temperature	90°C	85°C
	Plastic 2/	Supply Voltage	/3	
		Input Voltage	60%	
		Frequency	80%	
		Output Current	70%	
		Fanout	80%	
		Junction Temperature	70°C	
Bipolar	Plastic 1/	Supply Voltage	/3	/3
		Input Voltage	80%	70%
		Frequency	100%	90%
		Output Current	90%	80%
		Fanout	90%	80%
		Junction Temperature	90°C	85°C
	Plastic 2/	Supply Voltage	/3	
		Input Voltage	60%	
		Frequency	75%	
		Output Current	70%	
		Fanout	70%	
		Junction Temperature	70°C	

Table 2. Linear MOS and Bipolar Microcircuit Derating Guidelines

Type			Environment	
Digital	**Package**	**Derating Parameter**	**Protected**	**Normal**
MOS	Plastic 1/	Supply Voltage	/3	/3
		Frequency	90%	80%
		Output Current	90%	80%
		Fanout	100%	85%
		Junction Temperature	85°C	75°C
	Plastic 2/	Supply Voltage	/3	
		Frequency	80%	
		Output Current	70%	
		Fanout	80%	
		Junction Temperature	70°C	
Bipolar	Plastic 1/	Supply Voltage	/3	/3
		Frequency	80%	90%
		Output Current	75%	80%
		Fanout	75%	80%
		Junction Temperature	85°C	75°C
	Plastic 2/	Supply Voltage	/3	
		Frequency	75%	
		Output Current	70%	
		Fanout	70%	
		Junction Temperature	70°C	

Table 3. Microprocessor MOS and Bipolar Microcircuit Derating Guidelines

Type			Environment	
Digital	**Package**	**Derating Parameter**	**Protected**	**Normal**
MOS	Plastic 1/	Supply Voltage	/3	/3
		Frequency	100%	90%
		Output Current	90%	80%
		Junction Temperature	90°C	85°C
	Plastic 2/	Supply Voltage	/3	
		Frequency	80%	
		Output Current	70%	
		Junction Temperature	70°C	
Bipolar	Plastic 1/	Supply Voltage	/3	/3
		Frequency	100%	95%
		Output Current	90%	80%
		Junction Temperature	90°C	85°C
	Plastic 2/	Supply Voltage	/3	
		Frequency	80%	
		Output Current	70%	
		Junction Temperature	70°C	

Table 4. Microcircuit Memory MOS and Bipolar Microcircuit Derating Guidelines

Type			Environment	
GaAs	**Package**	**Derating Parameter**	**Protected**	**Normal**
Digital	Plastic 1/	Channel Temperature	125°C	90°C
	Plastic 2/	Channel Temperature	90°C	

Table 5. Digital MOS and Bipolar Microcircuit Derating Guidelines

Notes for Tables 1-5

Environmental Categories:

Protected Environment – applicable for parts employed according to the following conditions:

a. Used in readily accessible maintenance applications.
b. Used in a controlled environment.
c. Not used in an application with shock, vibration, pressure or moisture.
d. Not stored for later use.
e. With an application life span of up to 5 years.

Normal Environment – applicable for parts employed according to the following conditions:

a. used in inhabited applications
b. Used in applications usually accessible for maintenance or replacement.
c. Used in uncontrolled, but not extreme, temperature environment with a temperature range of -40°C to +85°C.
d. Can be stored for later usage (not exceed 10 years)
e. With an application life span of 5 to 10 years

1/ Plastic packaged microcircuit with heat dissipation mechanisms (e.g. thermal fillers, thermal conductivity plate or a type of metal substrate) built in.

2/ Low – power plastic packaged microcircuits with no heat dissipation mechanism other than through the leads.

3/ The supply voltage must be kept within the microcircuit specification sheets minimum and maximum limit.

APPENDIX C

STRESS ANALYSIS WORKSHEETS

System	Schematic Title:												Drawing No.			
	NEXT ASSY. TITLE:												DRAWING NO.			
Ref. Des. (Type)	Const- Ruction / Resistive Element	Package Type	Vendor	Procur. Part No.	Norm Resist	Mfg Tol	Ta 1/	Voltage Norm Rated	Voltage Actual	Power Dissipation Rated 25ºC	Power Dissipation Rated Max Amp	Power Dissipation Actual	Percent Power Rated	Percent Voltage Rated	Wave Form (dc, sine, pulse, etc)	REMARKS
					W	%	ºC	V	V	mW	mW	mW	%	V		
	REPORT NUM.	REV	DATE		PREPARED BY:			DATE		APPROVED BY			DATE	SHEET ______ OF ______		

TABLE 1: EXAMPLE PART USAGE AND APPLIED STRESS DATA CHART FOR RESISTORS

NOTES:

1/ AMBIENT TEMPERATURE

System						Schematic Title:							Drawing No.			
						NEXT ASSY. TITLE:							DRAWING NO.			
								VOLTAGE								
Ref. Des. #	Const. Dielec-tric	Cap Type	Vendor	Procur Doc	Part Amb. Temp	Mfg Tol	Cap Value	Rated Td 1/	DC	FREQ	PULSE PEAK	REP RATE	Percent Power Rated	Percent Voltage Rated	Wave Form (dc, sine, pulse, etc)	REMARKS
					ºC	%		V	VDC	KHz	V	Ms	%	V		
	REPORT NUM.	REV		DATE	PREPARED BY:			DATE		APPROVED BY			DATE	SHEET ______ OF ______		

TABLE 2. EXAMPLE PART USAGE AND APPLIED STRESS DATA CHART FOR CAPACITORS

NOTES:

1/ MAXIMUM DERATING TEMPERATURE

SYSTEM	SCHEMATIC TITLE:	DRAWING NO.
	NEXT ASSY. TITLE:	DRAWING NO.

Ref Des #	Ven -d Part #	Ven -d	Pro- c Doc	Type GP, power Etc.	Part Amb. Temp.		Contact Arrange- ment	Contact Loading						Coil Voltage						% Cont Power Rating
								Cont- act	Power		Current		Load	Max.		Pickup		Dropout		
					Norm Rated	act			Norm rated	act	Rated	act	Res/ ind cap	Norm rated	act	Rated	act	Norm rated	act	
					°C	°C			mW	mW	mA	mA		mV	mV	mV	mV	mV	mV	%

REPORT NUM. REV DATE	PREPARED BY: DATE	APPROVED BY DATE	SHEET ___________ OF ___________

TABLE 3. EXAMPLE PART USAGE AND APPLIED STRESS DATA CHART FOR RELAYS

System

Schematic Title: Drawing No.

NEXT ASSY. TITLE: DRAWING NO.

Ref. Des. #	Vendor Part #	Vendor	Proc. Part No	Type SI GE	Max Amb Temp	Peak Inverse Voltage		Forward Current		Voltage			Percent Current Rating	Percent PIV Rating	Tj	REMARKS
						Max Rated	Actual	Max Rated	Actial	Rated 25ºC	Rated Max Amp	Actual				
						V	V	mA	mA	V	V	V	%	%	°C	

REPORT NUM. REV DATE

PREPARED BY: DATE

APPROVED BY DATE

SHEET ___________ OF ___________

TABLE 4. EXAMPLE PART USAGE AND APPLIED STRESS DATA CHART FOR ZENER DIODES

System						Schematic Title:							Drawing No.		
						NEXT ASSY. TITLE:							DRAWING NO.		
Ref. Des. #	Vendor Part #	Vendor	Proc. Part No	Type SI GE	Max Amb Temp	Peak Inverse Voltage		Forward Current		Power DIssipation			Percent Current Rating	Percent PIV Rating	REMARKS
						Max Rated	Actual	Max Rated	Actial	Rated 25ºC	Rated Max Amp	Actual			
						V	V	A	A	mW	mW	mW	%	%	
REPORT NUM.	REV	DATE	PREPARED BY:		DATE					APPROVED BY		DATE	SHEET ______ OF ______		

TABLE 5. EXAMPLE PART USAGE AND APPLIED STRESS CHART FOR GENERAL PURPOSE AND POWER RECTIFIER DIODES

System	Schematic Title:	Drawing No.
	NEXT ASSY. TITLE:	DRAWING NO.

Ref. Des .#	Vend Part #	Vend	Proc Part No	Part amb temp	Power Dissipation			Voltage						Current			% outp. rating	% supp rating	% curr. rating	% Ic rating	Q Res	T j
					Rated		Act	Input		Output		Supply		Collector		% inp. rat-ing						
					@ 25°C	@ Td		rated	act	rated	act	rated	act	rated	act							
				°C	mW	mW	mW	V	V	V	V	V	V	mA	mA	%	%	%	%	%	°C/W	

REPORT NUM.	REV	DATE	PREPARED BY:	DATE	APPROVED BY	DATE	SHEET ___________ OF ___________

TABLE 6. EXAMPLE PART USAGE AND APPLIED STRESS DATA CHART FOR LINEAR MICROCIRCUITS

APPENDIX D:

TYPICAL PCB PART APPROVAL REQUEST FORM

<table>
<tr><th colspan="4">GLAST LAT PCB PART APPROVAL REQUEST</th></tr>
<tr><td colspan="2">1. Contract Number:</td><td colspan="2">2a. REQUEST Number:</td></tr>
<tr><td colspan="3">3. Project Name:</td><td>2b. Resubmittal: ☐</td></tr>
<tr><td colspan="4">4a. Contractor:</td></tr>
<tr><td colspan="4">4b. Subcontractor, vendor, or collaborator:</td></tr>
<tr><td colspan="4">5. System & Component:</td></tr>
<tr><td colspan="4">6. Part Name:</td></tr>
<tr><td colspan="2">7. Part Number:</td><td colspan="2">8. Commercial Part Number:</td></tr>
<tr><td colspan="3">9. Part Manufacturer:</td><td>FSCM:</td></tr>
<tr><td colspan="2">10. Procurement Spec.:</td><td colspan="2">Revision</td></tr>
<tr><td colspan="2">11. Screening Spec.:</td><td colspan="2">Revision</td></tr>
<tr><td colspan="4">12. Describe Critical Parameters:</td></tr>
<tr><td colspan="4">13. Justification for use of Requested Part:</td></tr>
<tr><td>14.</td><td>Approval Signatures</td><td>Title</td><td>Date</td></tr>
<tr><td colspan="4">Requested By:</td></tr>
<tr><td colspan="4">Reviewed By:</td></tr>
<tr><td colspan="4">Approved By:</td></tr>
<tr><td colspan="4">Approved By:</td></tr>
</table>

INSTRUCTIONS FOR ENTERING DATA ON PCB APPROVAL PARTS APPROVAL REQUEST FORMS

Block 1 - Enter the prime contract number

Block 2a - Enter the serial number to each REQUEST

Block 2b - If this REQUEST is being resubmitted as a result of prior disapproval, check this block.

Block 3 - Enter the Full Project Name

Block 4a - Enter the name of the prime contractor

Block 4b. - Enter the name of the subcontractor, vendor, or collaborator, if applicable

Block 5 - Enter the name of the system and component (BOX) in full for spacecraft systems.

- Enter the name of the experiment or instrument for payload items.

Block 6 - Enter in full, the name of the part; i.e., capacitor, resistor. (use listing in the GSFC preferred parts list PPL-21 as a guide). Multiple parts listings on a single REQUEST are not permitted.

Block 7 - Enter the part number, which uniquely identifies the part. If it is a mil part, enter the mil part number. If it is procured to a source control drawing (SCD), enter the SCD number and dash number associated with the source used. Otherwise use the commercial designation.

Block 8 - Enter the commercial number for the parts.

Block 9 - Enter in full, the name and location of the manufacturer of the part or device and/or the FSCM number. For non-standard MIL-Spec parts, the designation QPL may be used on lieu of manufacturer's identification if the actual source is not known. Multiple source listings may appear on a single request form.

Block 10 -Enter the procurement specification and appropriate revision letter to which the part or device is to be procured. If no procurement specification is used enter "Commercial". Attach one copy of applicable documents for review.

Block 11 - Enter the screening specification and appropriate revision letter to which the part or device is to be tested. Attach one copy of applicable documents for review.

Block 12 - Describe the critical parameters that dictate the use of this part.

Block 13 - Enter the basis for justification for the usage of the part. Indicate the qualification status of the part. The criterion for qualification by similarity includes similarity of design and function and includes fabrication by same manufacturer using the same process and quality controls as the standard part. If prior usage on NASA spacecraft is used as basis for acceptance, indicate the programs where used with launch dates and orbital life. The part application must be congruent with that used in prior programs. Attach on copy of the qualification test plan to be used if none of the above is applicable.

Block 14 - For PCB Request generated by the Engineer, enter the signature and title of the preparer, the parts/reliability engineer and the project program engineer or his/her designated representative. The signatures provide that appropriate personnel have reviewed the request and that the information included is accurate and complete.

APPENDIX E

PARTS IDENTIFICATION LIST (PIL)

Assembly	Procurement Part Number	Procurement Specification	Generic Part Number	Description	FSC Code	Recommended Supplier

Supplier CAGE Code	Quantity	Package Type	Package Designation	TID	SEE	Responsible Engineer

GFE	Approved	Assembly Number	Reference Designator	GIDEP OK	Date Code